查询M36W108AB100ZM1T供应商

M36W108AT
M36W108AB

8 Mbit (1Mb x8, Boot Block) Flash Memory and 1 Mbit (128Kb x8) SRAM Low Voltage Multi-Memory Product

PRELIMINARY DATA

- SUPPLY VOLTAGE
  - V_{CCF} = V_{CCS} = 2.7V to 3.6V: for Program, Erase and Read
- ACCESS TIME: 100ns
- LOW POWER CONSUMPTION
  - Read: 40mA max. (SRAM chip)
  - Stand-by: 30µA max. (SRAM chip)
  - Read: 10mA max. (Flash chip)
  - Stand-by: 100µA max. (Flash chip)

FLASH MEMORY

- 8 Mbit (1Mb x 8) BOOT BLOCK ERASE
- PROGRAMMING TIME: 10µs typical
- PROGRAM/ERASE CONTROLLER (P/E.C.)
  - Program Byte-by-Byte
  - Status Register bits and Ready/Busy Output
- SECURITY PROTECTION MEMORY AREA
- INSTRUCTION ADDRESS CODING: 3 digits
- MEMORY BLOCKS
  - Boot Block (Top or Bottom location)
  - Parameter and Main Blocks
- BLOCK, MULTI-BLOCK and CHIP ERASE
- ERASE SUSPEND and RESUME MODES
  - Read and Program another Block during Erase Suspend
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Device Code, M36W108AT: D2h
  - Device Code, M36W108AB: DCh

SRAM

- 1 Mbit (128Kb x 8)
- POWER DOWN FEATURES USING TWO CHIP ENABLE INPUTS
- LOW V_{CC} DATA RETENTION: 2V

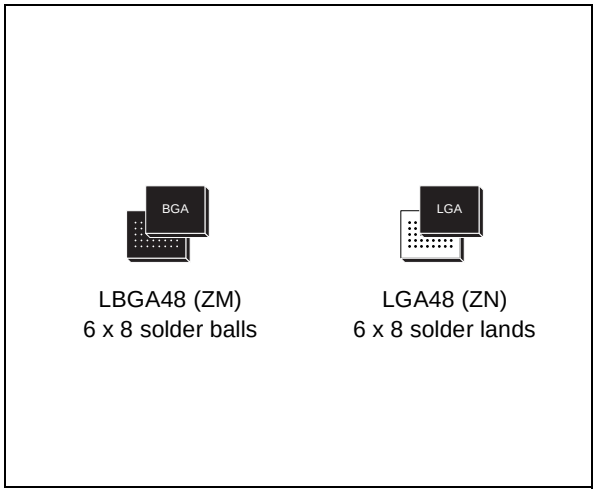
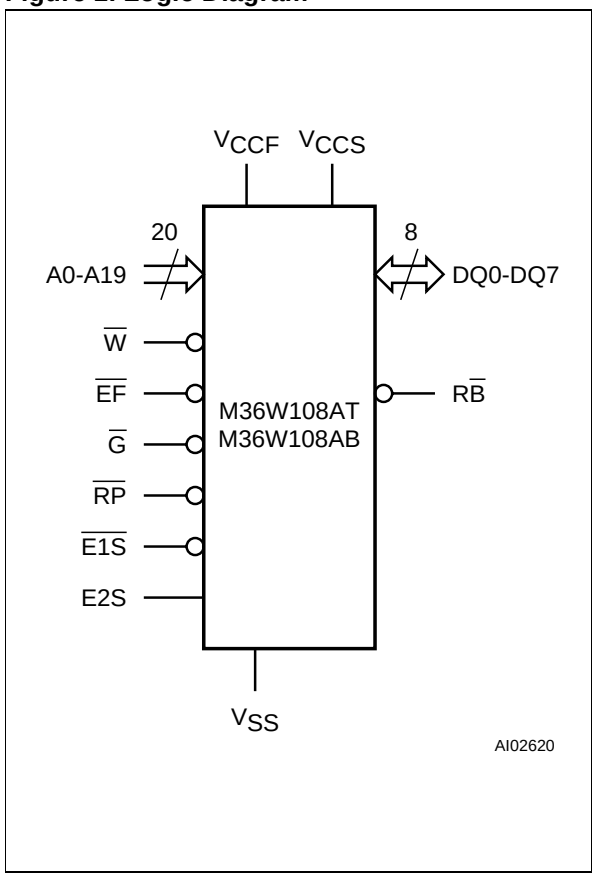


Figure 1. Logic Diagram



This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Figure 2. LBGA and LGA Connections (Top View)

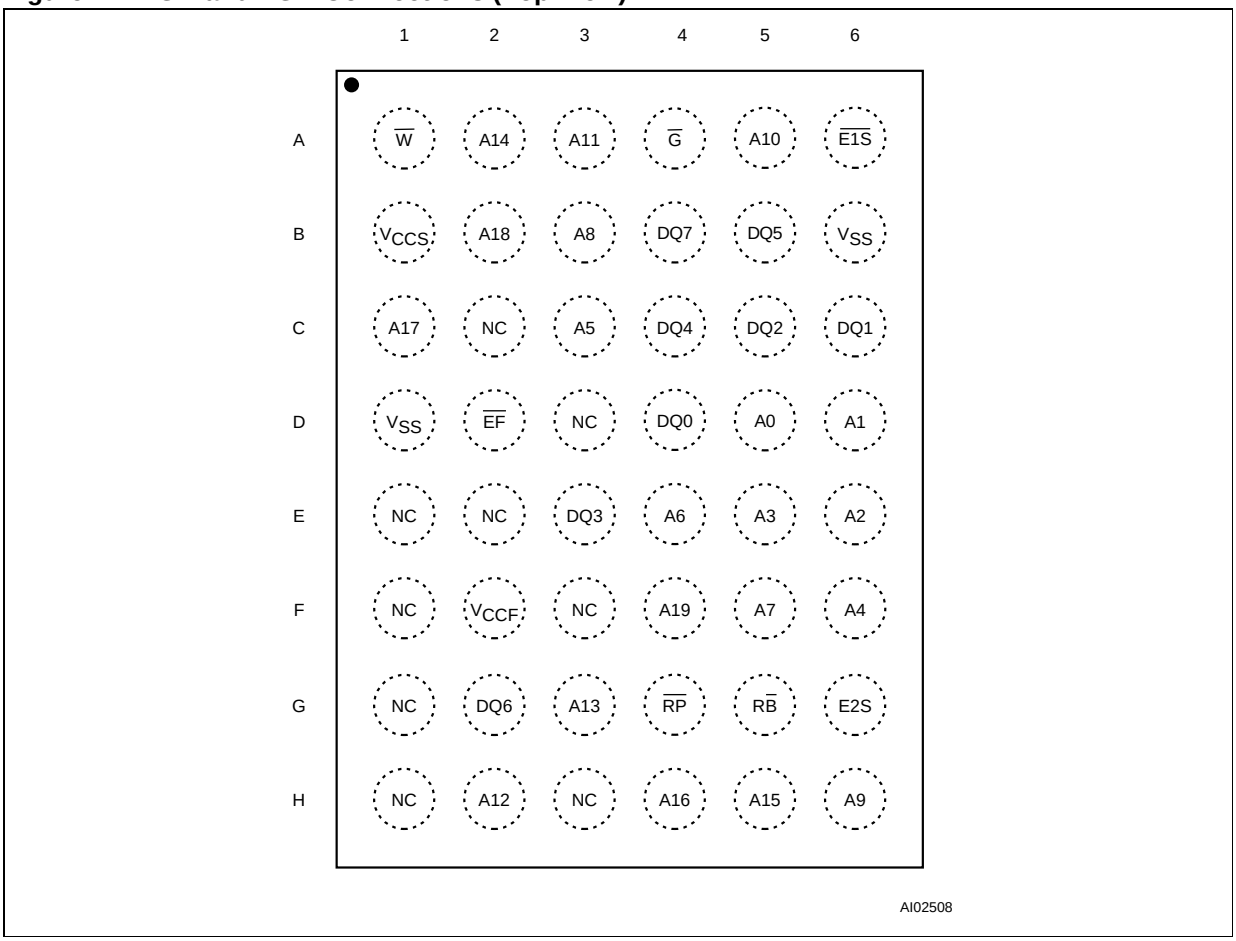

1 2 3 4 5 6
A W A14 A11 G A10 E1S
B VCCS A18 A8 DQ7 DQ5 VSS
C A17 NC A5 DQ4 DQ2 DQ1
D VSS EF NC DQ0 A0 A1
E NC NC DQ3 A6 A3 A2
F NC VCCF NC A19 A7 A4
G NC DQ6 A13 RP RB E2S
H NC A12 NC A16 A15 A9
AI02508

Table 1. Signal Names

A0-A16	Address Inputs
A17-A19	Address Inputs for Flash Chip
DQ0-DQ7	Data Input/Outputs, Command Inputs for Flash Chip
$\overline{EF}$	Chip Enable for Flash Chip
$\overline{E1S}$, E2S	Chip Enable for SRAM Chip
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset for Flash Chip
$R\overline{B}$	Ready/Busy Output for Flash Chip
V_{CCF}	Supply Voltage for Flash Chip
V_{CCS}	Supply Voltage for SRAM Chip
V_{SS}	Ground
NC	Not Connected Internally

DESCRIPTION

The M36W108A is multi-chip device containing an 8 Mbit boot block Flash memory and a 1 Mbit of SRAM. The device is offered in the new Chip Scale Package solutions: LBGA48 1.0mm ball pitch and LGA48 1.0mm land pitch.

The two components, of the package's overall 9 Mbit of memory, are distinguishable by use of the three chip enable lines: $\overline{EF}$ for the Flash memory, $\overline{E1S}$ and E2S for the SRAM.

The Flash memory component is identical with the M29W008A device. It is a non-volatile memory that may be erased electrically at the block or chip level and programmed in-system on a Byte-by-Byte basis using only a single 2.7V to 3.6V V_{CCF} supply. For Program and Erase operations the necessary high voltages are generated internally. The device can also be programmed in standard programmers. The array matrix organization allows each block to be erased and reprogrammed without affecting other blocks.

Instructions for Read/Reset, Auto Select for reading the Electronic Signature, Programming, Block

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (3)	–40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltage	–0.5 to V_{CC} +0.5	V
V_{CCF}	Flash Chip Supply Voltage	–0.6 to 5	V
V_{CCS}	SRAM Chip Supply Voltage	–0.3 to 4.6	V
$V_{(\overline{EF}, \overline{RP})}$	$\overline{EF}$, $\overline{RP}$ Voltage	0.6 to 13.5	V
PD	Power Dissipation	0.7	W

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.
3. Depends on range.

and Chip Erase, Erase Suspend and Resume are written to the device in cycles of commands to a Command Interface using standard microprocessor write timings.

The SRAM component is a low power SRAM that features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 2.7V to 3.6V V_{CCS} supply, and all inputs and outputs are TTL compatible.

SIGNAL DESCRIPTIONS

See Figure 1 and Table 1.

Address Inputs (A0-A16). Addresses A0 to A16 are common inputs for the Flash chip and the SRAM chip. The address inputs for the Flash memory or the SRAM array are latched during a write operation on the falling edge of Flash Chip Enable ($\overline{EF}$), SRAM Chip Enable ($\overline{E1S}$ or E2S) or Write Enable ($\overline{W}$).

Address Inputs (A17-A19). Address A17 to A19 are address inputs for the Flash chip. They are latched during a write operation on the falling edge of Flash Chip Enable ($\overline{EF}$) or Write Enable ($\overline{W}$).

Data Input/Outputs (DQ0-DQ7). The input is data to be programmed in the Flash or SRAM memory array or a command to be written to the C.I. of the Flash chip. Both are latched on the rising edge of Flash Chip Enable ($\overline{EF}$), SRAM Chip Enable ($\overline{E1S}$ or E2S) or Write Enable ($\overline{W}$). The output is data from the Flash memory or SRAM array, the Electronic Signature Manufacturer or Device codes or the Status register Data Polling bit DQ7, the Toggle Bits DQ6 and DQ2, the Error bit DQ5 or the Erase Timer bit DQ3. Outputs are valid when Flash Chip Enable ($\overline{EF}$) or SRAM Chip Enable ($\overline{E1S}$ or E2S) and Output Enable ($\overline{G}$) are active. The output is high impedance when the both the Flash chip and the SRAM chip are deselected or the outputs are disabled and when Reset ($\overline{RP}$) is at a V_{IL}.

Flash Chip Enable ($\overline{EF}$). The Chip Enable input for Flash activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{EF}$ at V_{IH} deselects the memory and reduces the power consumption to the standby level. $\overline{EF}$ can also be used to control writing to the command register and to the Flash memory array, while $\overline{W}$ remains at V_{IL}. It is not allowed to set $\overline{EF}$ at V_{IL}, $\overline{E1S}$ at V_{IL} and E2S at V_{IH} at the same time.

SRAM Chip Enable ($\overline{E1S}$, E2S). The Chip Enable inputs for SRAM activate the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E1S}$ at V_{IH} or E2S at V_{IL} deselects the memory and reduces the power consumption to the standby level. $\overline{E1S}$ and E2S can also be used to control writing to the SRAM memory array, while $\overline{W}$ remains at V_{IL}. It is not allowed to set $\overline{EF}$ at V_{IL}, $\overline{E1S}$ at V_{IL} and E2S at V_{IH} at the same time.

Output Enable ($\overline{G}$). The Output Enable gates the outputs through the data buffers during a read operation. When $\overline{G}$ is High the outputs are High impedance.

Write Enable ($\overline{W}$). The Write Enable input controls writing to the Command Register of the Flash chip and Address/Data latches.

Table 3. Main Operation Modes (1)

Operation Mode	$\overline{EF}$	$\overline{E1S}$	E2S	$\overline{G}$	$\overline{W}$	$\overline{RP}$	DQ7-DQ0
Flash Chip Read	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	V_{IH}	Data Output
	V_{IL}	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Data Output
SRAM Chip Read	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	Data Output
Flash Chip Write	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	V_{IH}	Data Input
	V_{IL}	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Data Input
SRAM Chip Write	V_{IH}	V_{IL}	V_{IH}	X	V_{IL}	X	Data Input
Flash Chip Output Disable	X	V_{IH}	X	V_{IH}	V_{IH}	X	Hi-Z
	X	X	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
SRAM Chip Output Disable	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Hi-Z
Flash Chip Stand-by	V_{IH}	X	X	X	X	V_{IH}	Hi-Z
Flash Chip Reset	X	V_{IH}	X	X	X	V_{IL}	Hi-Z
	X	X	V_{IL}	X	X	V_{IL}	Hi-Z
SRAM Chip Stand-by	X	V_{IH}	X	X	X	V_{IL}	Hi-Z
	X	X	V_{IL}	X	X	V_{IL}	Hi-Z

Note: 1. X = V_{IL} or V_{IH}.

Reset Input ($\overline{RP}$). The Reset input provides hardware reset of the Flash chip. Reset of the Flash memory is achieved by pulling $\overline{RP}$ to V_{IL} for at least t_{PLPX}. When the reset pulse is given, if the Flash memory is in Read or Standby modes, it will be available for new operations in t_{PHEL} after the rising edge of $\overline{RP}$.

If the Flash memory is in Erase or Program mode the reset will take t_{PLYH} during which the Ready/Busy ($\overline{RB}$) signal will be held at V_{IL}. The end of the Flash memory reset will be indicated by the rising edge of $\overline{RB}$. A hardware reset during an Erase or Program operation will corrupt the data being programmed or the block(s) being erased. See Table 18 and Figure 10.

Ready/Busy Output ($\overline{RB}$). Ready/Busy is an open-drain output of the Flash chip. It gives the internal state of the Program/Erase Controller (P/E.C.) of the Flash device. When $\overline{RB}$ is Low, the Flash device is busy with a Program or Erase operation and it will not accept any additional program or erase instructions except the Erase Suspend instruction. When $\overline{RB}$ is High, the Flash device is ready for any Read, Program or Erase operation. The $\overline{RB}$ will also be High when the Flash memory is put in Erase Suspend or Standby modes.

V_{CCF} Supply Voltage. Flash memory power supply for all operations (Read, Program and Erase).

V_{CCS} Supply Voltage. SRAM power supply for all operations (Read, Program).

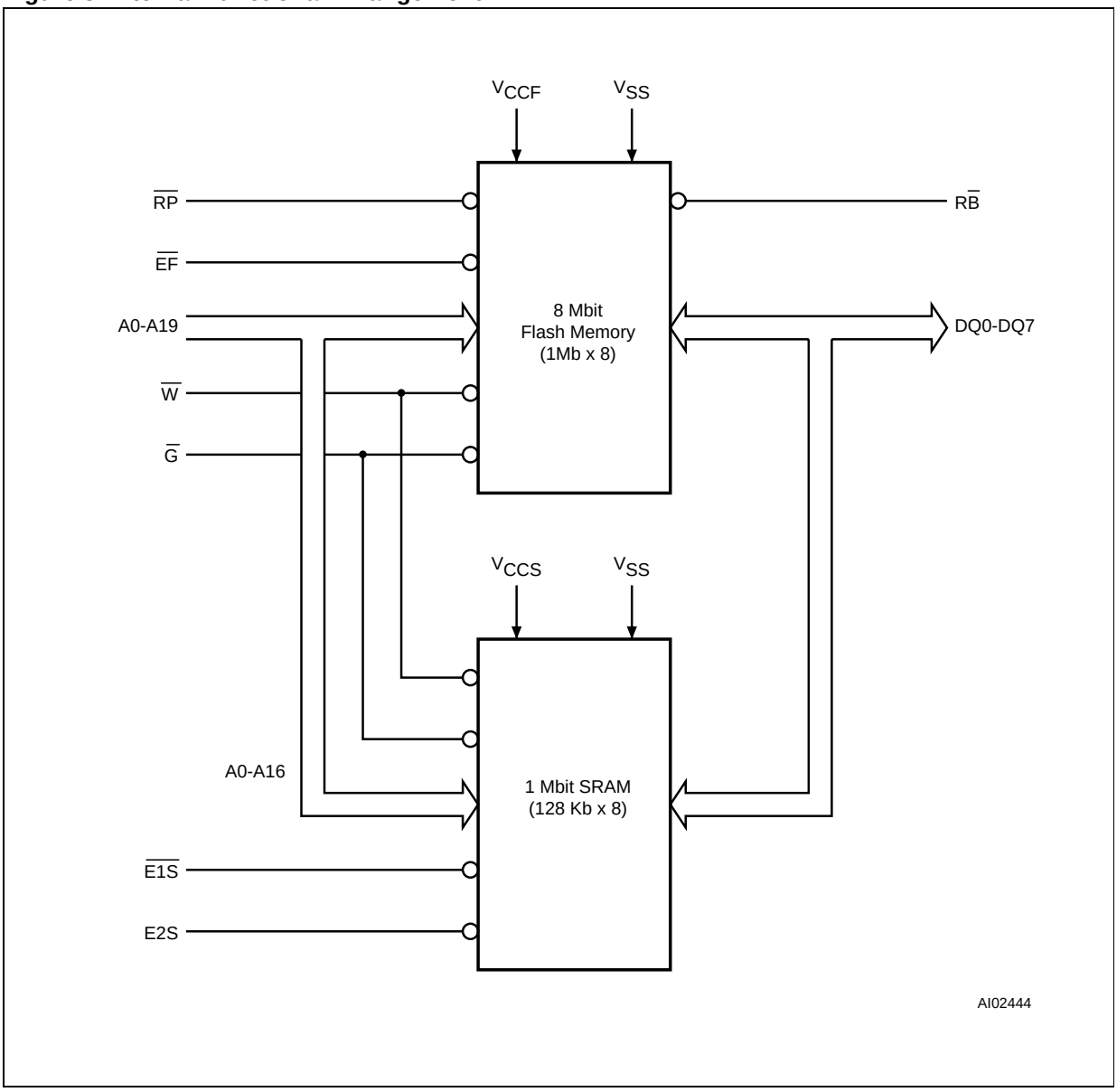
V_{SS} Ground. V_{SS} is the reference for all voltage measurements.

POWER SUPPLY

Power Up. The Flash memory Command Interface is reset on power up to Read Array. Either Flash Chip Enable ($\overline{EF}$) or Write Enable ($\overline{W}$) inputs must be tied to V_{IH} during Power Up to allow maximum security and the possibility to write a command on the first rising edge of $\overline{EF}$ and $\overline{W}$. Any write cycle initiation is blocked when V_{CCF} is below V_{LKO}.

Supply Rails. Normal precautions must be taken for supply voltage decoupling; each device in a system should have the V_{CCF}, V_{CCS} rails decoupled with a 0.1µF capacitor close to the V_{CCF}, V_{CCS} and V_{SS} pins. The PCB trace widths should be sufficient to carry the V_{CCF} and V_{CCS} program currents and the V_{CCF} erase current required.

Figure 3. Internal Functional Arrangement



FLASH MEMORY COMPONENT

Organization and Architecture

Organization. The Flash chip is organized as 1Mbit x 8. The memory uses the address inputs A0-A19 and the Data Input/Outputs DQ0-DQ7. Memory control is provided by Chip Enable ($\overline{E}$), Output Enable ($\overline{G}$) and Write Enable ($\overline{W}$) inputs.

Erase and Program operations are controlled by an internal Program/Erase Controller (P/E.C.). Status Register data output on DQ7 provides a Data Polling signal, while Status Register data outputs on DQ6 and DQ2 provide Toggle signals to indicate the state of the P/E.C. operations. A Ready/Busy ($\overline{RB}$) output indicates the completion of the internal algorithms.

Memory Blocks. The device features asymmetrically blocked architecture providing system memory integration. Both Top and Bottom Boot Block devices have an array of 19 blocks, one Boot Block of 16K Bytes, two Parameter Blocks of 8K Bytes, one Main Block of 32K Bytes and fifteen Main Blocks of 64K Bytes. The Top Boot Block version has the Boot Block at the top of the memory address space and the Bottom Boot Block version locates the Boot Block starting at the bottom. The memory maps and block address tables are showed in Figures 4, 5 and Tables 4, 5. Each block can be erased separately, any combination of blocks can be specified for multi-block erase or the entire chip may be erased. The Erase operations are managed automatically by the P/E.C. The block erase operation can be suspended in order to read from or program to any block not being erased, and then resumed.

Device Operations

The following operations can be performed using the appropriate bus cycles: Read Array, Write command, Output Disable, Standby and Reset (see Table 6).

Read. Read operations are used to output the contents of the Memory Array, the Electronic Signature or the Status Register. Both Chip Enable ($\overline{E}$) and Output Enable ($\overline{G}$) must be low, with Write Enable ($\overline{W}$) high, in order to read the output of the memory.

Table 4. Top Boot Block, Flash Block Address

Size (KWord)	Address Range
16	FC000h-FFFFFh
8	FA000h-FBFFFh
8	F8000h-F9FFFh
32	F0000h-F7FFFh
64	E0000h-EFFFFh
64	D0000h-DFFFFh
64	C0000h-CFFFFh
64	B0000h-BFFFFh
64	A0000h-AFFFFh
64	90000h-9FFFFh
64	80000h-8FFFFh
64	70000h-7FFFFh
64	60000h-6FFFFh
64	50000h-5FFFFh
64	40000h-4FFFFh
64	30000h-3FFFFh
64	20000h-2FFFFh
64	10000h-1FFFFh
64	00000h-0FFFFh

Table 5. Bottom Boot Block, Flash Block Address

Size (KWord)	Address Range
64	F0000h-FFFFFh
64	E0000h-EFFFFh
64	D0000h-DFFFFh
64	C0000h-CFFFFh
64	B0000h-BFFFFh
64	A0000h-AFFFFh
64	90000h-9FFFFh
64	80000h-8FFFFh
64	70000h-7FFFFh
64	60000h-6FFFFh
64	50000h-5FFFFh
64	40000h-4FFFFh
64	30000h-3FFFFh
64	20000h-2FFFFh
64	10000h-1FFFFh
32	08000h-0FFFFh
8	06000h-07FFFh
8	04000h-05FFFh
16	00000h-03FFFh

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable ($\overline{E}$) is Low and Write Enable ($\overline{W}$) is at V_{IL} with Output Enable ($\overline{G}$) at V_{IH}. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ whichever occurs last. Commands and Input Data are latched on the rising edge of $\overline{W}$ or $\overline{E}$ whichever occurs first.

Output Disable. The data outputs are high impedance when the Output Enable ($\overline{G}$) is at V_{IH} with Write Enable ($\overline{W}$) at V_{IH}.

Standby. The memory is in standby when Chip Enable ($\overline{E}$) is at V_{IH} and the P/E.C. is idle. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable ($\overline{G}$) or Write Enable ($\overline{W}$) inputs.

Automatic Standby. After 150ns of bus inactivity and when CMOS levels are driving the addresses, the chip automatically enters a pseudo-standby mode where consumption is reduced to the CMOS standby value, while outputs still drive the bus.

Instructions and Commands

Seven instructions are defined (see Table 7) to perform Read Array, Auto Select (to read the Electronic Signature), Program, Block Erase, Chip Erase, Erase Suspend and Erase Resume. The internal P/E.C. automatically handles all timing and verification of the Program and Erase operations. The Status Register Data Polling, Toggle, Error bits and the $\overline{RB}$ output may be read at any time, during programming or erase, to monitor the progress of the operation.

Instructions, made up of commands written in cycles, can be given to the Program/Erase Controller through a Command Interface (C.I.).

The C.I. latches commands written to the memory. Commands are made of address and data sequences. Two coded cycles unlock the Command Interface. They are followed by an input command or a confirmation command. The coded sequence consists of writing the data AAh at the address 5555h during the first cycle and the data 55h at the address 2AAAh during the second cycle.

Table 6. Flash User Bus Operations (1)

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	A15	A12	A9	A6	A1	A0	DQ7-DQ0
Read Byte	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A15	A12	A9	A6	A1	A0	Data Output
Write Byte	V_{IL}	V_{IH}	V_{IL}	V_{IH}	A15	A12	A9	A6	A1	A0	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	X	X	X	Hi-Z
Stand-by	V_{IH}	X	X	V_{IH}	X	X	X	X	X	X	Hi-Z
Reset	X	X	X	V_{IL}	X	X	X	X	X	X	Hi-Z

Note: 1. X = V_{IL} or V_{IH}.

Table 7. Read Flash Electronic Signature

Code	Device	$\overline{E}$	$\overline{G}$	$\overline{W}$	A1	A0	Other Addresses	DQ7-DQ0
Manufact. Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Don't care	20h
Device Code	M36W108AT	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Don't care	D2h
	M36W108AB	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Don't care	DCh

Table 8. Flash Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Chip Erase Confirm
20h	Reserved
30h	Block Erase Resume/Confirm
80h	Set-up Erase
90h	Read Electronic Signature/ Block Protection Status
A0h	Program
B0h	Erase Suspend
F0h	Read Array/Reset

Instructions are composed of up to six cycles. The first two cycles input a Coded Sequence to the Command Interface which is common to all instructions (see Table 9). The third cycle inputs the instruction set-up command. Subsequent cycles output the addressed data or Electronic Signature for Read operations. In order to give additional data protection, the instructions for Program and Block or Chip Erase require further command inputs. For a Program instruction, the fourth command cycle inputs the address and data to be programmed. For an Erase instruction (block or chip), the fourth and fifth cycles input a further Coded Sequence before the Erase confirm command on the sixth cycle. Erasure of a memory block may be suspended, in order to read data from another block or to program data in another block, and then resumed.

When power is first applied or if V_{CCF} falls below V_{LKO}, the command interface is reset to Read Array. Command sequencing must be followed exactly. Any invalid combination of commands will reset the device to Read Array. The increased number of cycles has been chosen to assure maximum data security.

Read/Reset (RD) Instruction. The Read/Reset instruction consists of one write cycle giving the command F0h. It can be optionally preceded by the two Coded cycles. Subsequent read operations will read the memory array addressed and output the data read. A wait state of t_{PLYH} is necessary after Read/Reset prior to any valid read if the memory was in an Erase or Program mode when the RD instruction is given (see Table 18 and Figure 10).

Auto Select (AS) Instruction. This instruction uses the two Coded cycles followed by one write cycle giving the command 90h to address 5555h for command set-up. A subsequent read will output the Manufacturer Code or the Device Code (Electronic Signature) depending on the levels of A0 and A1 (see Table 7). The Electronic Signature can be read from the memory allowing programming equipment or applications to automatically match their interface to the characteristics of the Flash memory. The Manufacturer Code, 20h, is output when the addresses lines A0 and A1 are at V_{IL}, the Device Code is output when A0 is at V_{IH} with A1 at V_{IL}. Other address inputs are ignored.

Program (PG) Instruction. This instruction uses four write cycles. The Program command A0h is written to address 5555h on the third cycle after two Coded Cycles. A fourth write operation latches the Address and the Data to be written and starts the P/E.C. Read operations output the Status Register bits after the programming has started. Memory programming is made only by writing '0' in place of '1'. Status bits DQ6 and DQ7 determine if programming is on-going and DQ5 allows verification of any possible error. Programming at an address not in blocks being erased is also possible during erase suspend. In this case, DQ2 will toggle at the address being programmed.

Block Erase (BE) Instruction. This instruction uses a minimum of six write cycles. The Erase Set-up command 80h is written to address 5555h on third cycle after the two Coded cycles. The Block Erase Confirm command 30h is similarly written on the sixth cycle after another two Coded Cycles. During the input of the second command an address within the block to be erased is given and latched into the memory.

Additional block Erase Confirm commands and block addresses can be written subsequently to erase other blocks in parallel, without further Coded cycles. The erase will start after the erase timeout period (see Erase Timer Bit DQ3 description). Thus, additional Erase Confirm commands for other blocks must be given within this delay. The input of a new Erase Confirm command will restart the timeout period. The status of the internal timer can be monitored through the level of DQ3, if DQ3 is '0' the Block Erase Command has been given and the timeout is running, if DQ3 is '1', the timeout has expired and the P/E.C. is erasing the block(s). If the second command given is not an erase confirm or if the Coded cycles are wrong, the instruction aborts, and the device is reset to Read Array. It is not necessary to program the block with 00h as the P/E.C. will do this automatically before to erasing to FFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{EF}$ output the Status Register bits.

During the execution of the erase by the P/E.C., the memory only accepts the Erase Suspend (ES) and Read/Reset (RD) instructions. A Read/Reset command will definitively abort erasure and result in invalid data in blocks being erased. A complete state of the block erase operation is given by the Status Register bits (see DQ2, DQ3, DQ5, DQ6 and DQ7 description).

Chip Erase (CE) Instruction. This instruction uses six write cycles. The Erase Set-up command 80h is written to address 5555h on the third cycle after the two Coded Cycles. The Chip Erase Confirm command 10h is similarly written on the sixth cycle after another two Coded Cycles. If the second command given is not an erase confirm or if the Coded Sequence is wrong, the instruction aborts and the device is reset to Read Array. It is not necessary to program the array with 00h first as the P/E.C. will automatically do this before erasing it to FFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{EF}$ output the Status Register bits. A complete state of the chip erase operation is given by the Status Register bits (see DQ2, DQ3, DQ5, DQ6 and DQ7 description).

Erase Suspend (ES) Instruction. The Block Erase operation may be suspended by this instruction which consists of writing the command B0h without any specific address. No Coded Cycles are required. It permits reading of data from another block and programming in another block while an erase operation is in progress. Erase suspend is accepted only during the Block Erase instruction execution. Writing this command during the erase timeout period will, in addition to suspending the erase, terminate the timeout. The Toggle bit DQ6 stops toggling when the P/E.C. is suspended. The Toggle bits will stop toggling between 0.1µs and 15µs after the Erase Suspend (ES) command has been written. The device will then automatically be set to Read Memory Array mode. When erase is suspended, a Read from blocks being erased will output DQ2 toggling and DQ6 at '1'. A Read from a block not being erased returns valid data. During suspension the memory will respond only to the Erase Resume (ER) and the Program (PG) instructions. A Program operation can be initiated during Erase Suspend in one of the blocks not being erased. It will result in both DQ2 and DQ6 toggling when the data is being programmed. A Read/Reset command will definitively abort erasure and result in invalid data in the blocks being erased.

Erase Resume (ER) Instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 30h, at any address, and without any Coded cycles.

Table 9. Flash Instructions (1)

Mne.	Instr.	Cyc.		1st Cyc.	2nd Cyc.	3rd Cyc.	4th Cyc.	5th Cyc.	6th Cyc.	7th Cyc.
RD (2,4)	Read/Reset Memory Array	1+	**Addr.** (3,6)	X	Read Memory Array until a new write cycle is initiated.					
			Data	F0h						
		3+	**Addr.** (3,6)	555h	2AAh	555h	Read Memory Array until a new write cycle is initiated.			
			Data	AAh	55h	F0h				
AS (4)	Auto Select	3+	**Addr.** (3,6)	555h	2AAh	555h	Read Electronic Signature until a new write cycle is initiated. See Note 5.			
			Data	AAh	55h	90h				
PG	Program	4	**Addr.** (3,6)	555h	2AAh	555h	Program Address	Read Data Polling or Toggle Bit until Program completes.		
			Data	AAh	55h	A0h	Program Data			
BE	Block Erase	6	**Addr.** (3,6)	555h	2AAh	555h	555h	2AAh	Block Address	Additional Block (7)
			Data	AAh	55h	80h	AAh	55h	30h	30h
CE	Chip Erase	6	**Addr.** (3,6)	555h	2AAh	555h	555h	2AAh	555h	Note 8
			Data	AAh	55h	80h	AAh	55h	10h	
ES (9)	Erase Suspend	1	**Addr.** (3,6)	X	Read until Toggle stops, then read all the data needed from any Block(s) not being erased then Resume Erase.					
			Data	B0h						
ER	Erase Resume	1	**Addr.** (3,6)	X	Read Data Polling or Toggle Bits until Erase completes or Erase is suspended another time.					
			Data	30h						

Note: 1. Commands not interpreted in this table will default to read array mode.
2. A wait of t_{PLYH} is necessary after a Read/Reset command if the memory was in an Erase, Erase Suspend or Program mode before starting any new operation (see Table 15 and Figure 8).
3. X = Don't care.
4. The first cycles of the RD or AS instructions are followed by read operations. Any number of read cycles can occur after the command cycles.
5. Signature Address bits A0, A1, at V_{IL} will output Manufacturer code (20h). Address bits A0 at V_{IH} and A1, at V_{IL} will output Device code.
6. For Coded cycles address inputs A11-A19 are don't care.
7. Optional, additional Blocks addresses must be entered within the erase timeout delay after last write entry, timeout status can be verified through DQ3 value (see Erase Timer Bit DQ3 description). When full command is entered, real Data Polling or Toggle bit until Erase is completed or suspended.
8. Read Data Polling, Toggle bits or $R\overline{B}$ until Erase completes.
9. During Erase Suspend, Read and Data Program functions are allowed in blocks not being erased.

Table 10. Flash Status Register Bits (1)

DQ	Name	Logic Level	Definition	Note
7	Data Polling	'1'	Erase Complete or erase block in Erase Suspend	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.
		'0'	Erase On-going	
		DQ	Program Complete or data of non erase block during Erase Suspend	
		$\overline{DQ}$	Program On-going	
6	Toggle Bit	'-1-0-1-0-1-0-1-'	Erase or Program On-going	Successive reads output complementary data on DQ6 while Programming or Erase operations are on-going. DQ6 remains at constant level when P/E.C. operations are completed or Erase Suspend is acknowledged.
		DQ	Program Complete	
		'-1-1-1-1-1-1-1-'	Erase Complete or Erase Suspend on currently addressed block	
5	Error Bit	'1'	Program or Erase Error	This bit is set to '1' in the case of Programming or Erase failure.
		'0'	Program or Erase On-going	
4	Reserved			
3	Erase Time Bit	'1'	Erase Timeout Period Expired	P/E.C. Erase operation has started. Only possible command entry is Erase Suspend (ES).
		'0'	Erase Timeout Period On-going	An additional block to be erased in parallel can be entered to the P/E.C.
2	Toggle Bit	'-1-0-1-0-1-0-1-'	Chip Erase, Erase or Erase Suspend on the currently addressed block. Erase Error due to the currently addressed block (when DQ5 = '1')	Indicates the erase status and allows to identify the erased block.
		'1'	Program on-going, Erase on-going on another block or Erase Complete	
		DQ	Erase Suspend read on non Erase Suspend block	
1	Reserved			
0	Reserved			

Note: 1. Logic level '1' is High, '0' is Low. -0-1-0-0-0-1-1-1-0- represent bit value in successive Read operations.

Table 11. Flash Polling and Toggle Bits (1)

Mode	DQ7	DQ6	DQ2
Program	$\overline{DQ7}$	Toggle	1
Erase	0	Toggle	Note 1
Erase Suspend Read (in Erase Suspend block)	1	1	Toggle
Erase Suspend Read (outside Erase Suspend block)	DQ7	DQ6	DQ2
Erase Suspend Program	$\overline{DQ7}$	Toggle	N/A

Note: 1. Toggle if the address is within a block being erased. '1' if the address is within a block not being erased.

Status Register Bits

P/E.C. status is indicated during execution by Data Polling on DQ7, detection of Toggle on DQ6 and DQ2, or Error on DQ5 and Erase Timer DQ3 bits. Any read attempt during Program or Erase command execution will automatically output these five Status Register bits. The P/E.C. automatically sets bits DQ2, DQ3, DQ5, DQ6 and DQ7. Other bits (DQ0, DQ1 and DQ4) are reserved for future use and should be masked (see Table 10 and Table 11).

Data Polling Bit (DQ7). When Programming operations are in progress, this bit outputs the complement of the bit being programmed on DQ7. During Erase operation, it outputs a '0'. After completion of the operation, DQ7 will output the bit last programmed or a '1' after erasing. Data Polling is valid and only effective during P/E.C. operation, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for erase. It must be performed at the address being programmed or at an address within the block being erased. If all the blocks selected for erasure are protected, DQ7 will be set to '0' for about 100µs, and then return to the previous addressed memory data value. See Figure 10 for the Data Polling flowchart and Figure 12 for the Data Polling waveforms. DQ7 will also flag the Erase Suspend mode by switching from '0' to '1' at the start of the Erase Suspend. In order to monitor DQ7 in the Erase Suspend mode an address within a block being erased must be provided. For a Read Operation in Erase Suspend mode, DQ7 will output '1' if the read is attempted on a block being erased and the data value on other blocks. During Program operation in Erase Suspend Mode, DQ7 will have the same behaviour as in the normal program execution outside of the suspend mode.

Toggle Bit (DQ6). When Programming or Erasing operations are in progress, successive attempts to read DQ6 will output complementary data. DQ6 will toggle following toggling of either $\overline{G}$, or $\overline{EF}$ when $\overline{G}$ is at V_{IL}. The operation is completed when two successive reads yield the same output data. The next read will output the bit last programmed or a '1' after erasing. The toggle bit DQ6 is valid only during P/E.C. operations, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for Erase. If the blocks selected for erasure are protected, DQ6 will toggle for about 100µs and then return back to Read. DQ6 will be set to '1' if a Read operation is attempted on an Erase Suspend block. When erase is suspended DQ6 will toggle during programming operations in a block different to the block in Erase Suspend. Either $\overline{EF}$ or $\overline{G}$ toggling will cause DQ6 to toggle. See Figure 12 for Toggle Bit flowchart and Figure 15 for Toggle Bit waveforms.

Toggle Bit (DQ2). This toggle bit, together with DQ6, can be used to determine the device status during the Erase operations. It can also be used to identify the block being erased. During Erase or Erase Suspend a read from a block being erased will cause DQ2 to toggle. A read from a block not being erased will set DQ2 to '1' during erase and to DQ2 during Erase Suspend. During Chip Erase a read operation will cause DQ2 to toggle as all blocks are being erased. DQ2 will be set to '1' during program operation and when erase is complete. After erase completion and if the error bit DQ5 is set to '1', DQ2 will toggle if the faulty block is addressed.

Error Bit (DQ5). This bit is set to '1' by the P/E.C. when there is a failure of programming, block erase, or chip erase that results in invalid data in the memory block. In case of an error in block erase or program, the block in which the error occurred or to which the programmed data belongs, must be discarded. The DQ5 failure condition will also appear if a user tries to program a '1' to a location that is previously programmed to '0'. Other Blocks may still be used. The error bit resets after a Read/Reset (RD) instruction. In case of success of Program or Erase, the error bit will be set to '0'.

Erase Timer Bit (DQ3). This bit is set to '0' by the P/E.C. when the last block Erase command has been entered to the Command Interface and it is awaiting the Erase start. When the erase timeout period is finished, after 50µs to 90µs, DQ3 returns to '1'.

Table 12. Flash Program/Erase Times and Endurance
(T_A = 0 to 70 °C; V_{CC} = 2.7 V to 3.6 V)

Parameter	Flash Memory Chip				Unit
	Min	Typ	Typical after 100k W/E Cycles	Max	
Chip Erase (Preprogrammed)		5	3.3		sec
Chip Erase		12			sec
Boot Block Erase		2.4			sec
Parameter Block Erase		2.3			sec
Main Block (32Kb) Erase		2.7			sec
Main Block (64Kb) Erase		3.3		15	sec
Chip Program (Byte)		8	8		sec
Byte Program		10	10		µs
Program/Erase Cycles (per Block)	100,000				cycles

SECURITY PROTECTION MEMORY AREA

The M36W108A features a security protection memory area. It consists of a memory block of 256 bytes or 128 words which is programmed in the ST factory to store a unique code that uniquely identifies the part.

This memory block can be read by using the Read Security Data instruction (RDS) as shown in Table 13.

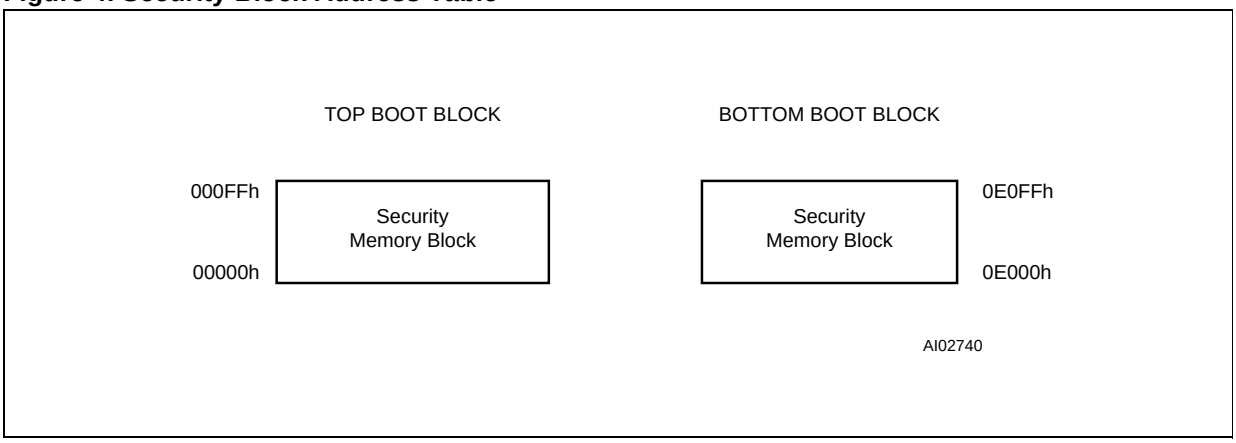
Read Security Data (RDS) Instruction. This RDS uses a single write cycle instruction: the command B8h is written to the adrress AAh. This sets the memory to the Read Security mode. Any successive read attempt will output the addressed Security byte until a new write cycle is initiated.

Table 13. Security Block Instruction

Mne.	Instr.	Cyc.		Unlock Cycle	2nd Cyc.
				1st Cyc.	
RDS	Read Security Data	1	**Addr.** (1)	AAh	Read OTP Data until a new write cycle is initiated
			Data (2)	B8h	

Note: 1. Address bits A10-A19 are don't care for coded address inputs.
2. Data bits DQ8-DQ15 are don't care for coded address inputs.

Figure 4. Security Block Address Table



SRAM COMPONENT

Device Operations

The following operations can be performed using the appropriate bus cycles: Read Array, Write Array, Output Disable, Power Down (see Table 14).

Read. Read operations are used to output the contents of the SRAM Array. The SRAM is in Read mode whenever Write Enable ($\overline{W}$) is at V_{IH} with Output Enable ($\overline{G}$) at V_{IL}, and both Chip Enables ($\overline{E1S}$ and E2S) are asserted.

Valid data will be available at the eight output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low, $\overline{E1S}$ is Low and E2S is High. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV}, t_{E2HQV}, or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{E1LQX}, t_{E2HQX} and t_{GLQX}, but data lines will always be valid at t_{AVQV} (see Table 22, Figure 15, Figure 16).

Write. Write operations are used to write data in the SRAM. The SRAM is in Write mode whenever the $\overline{W}$ and $\overline{E1S}$ pins are at V_{IL}, with E2S at V_{IH}. Either the Chip Enable inputs ($\overline{E1S}$ and E2S) or the Write Enable input ($\overline{W}$) must be de-asserted during address transitions for subsequent write cycles. Write begins with the concurrence of both Chip Enables being active with $\overline{W}$ at V_{IL}. A Write begins at the latest transition among $\overline{E1S}$ going to V_{IL}, E2S going to V_{IH} and $\overline{W}$ going to V_{IL}. Therefore, address setup time is referenced to Write Enable and both Chip Enables as t_{AVWL}, t_{AVE1L} and t_{AVE2H} respectively, and is determined by the latter occurring edge. The Write cycle can be terminated by the rising edge of $\overline{E1S}$, the rising edge of $\overline{W}$ or the falling edge of E2S, whichever occurs first.

If the Output is enabled ($\overline{E1S}$=V_{IL}, E2S=V_{IH} and $\overline{G}$=V_{IL}), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVE1H} before the rising edge of $\overline{E1S}$ or for t_{DVE2L} before the falling edge of E2S, whichever occurs first, and remain valid for t_{WHDX}, t_{E1HDX} or t_{E2LDX} (see Table 23, Figures 18, 19, 20).

Output Disable. The data outputs are high impedance when the Output Enable ($\overline{G}$) is at V_{IH} with Write Enable ($\overline{W}$) at V_{IH}.

Power-Down. The SRAM chip has a Chip Enable power-down feature which invokes an automatic standby mode (see Table 22, Figure 17) whenever either Chip Enable is de-asserted (E1S=V_{IH} or E2S=V_{IL}).

Data Retention

The SRAM data retention performances as V_{CCS} go down to V_{DR} are described in Table 23 and Figures 22, 23. In $\overline{E1S}$ controlled data retention mode, minimum standby current mode is entered when $\overline{E1S} \geq V_{CCS} - 0.2V$ and $E2S \leq 0.2V$ or $E2S \geq V_{CCS} - 0.2V$. In E2S controlled data retention mode, minimum standby current mode is entered when $E2S \leq 0.2V$.

Table 14. SRAM User Bus Operations (1)

Operation	$\overline{E1S}$	E2S	$\overline{W}$	$\overline{G}$	DQ7-DQ0	Power
Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Data Output	Active
Write	V_{IL}	V_{IH}	V_{IL}	X	Data Input	Active
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z	Active
Power Down	V_{IH}	X	X	X	Hi-Z	Stand-by TTL
	X	V_{IL}	X	X	Hi-Z	Stand-by TTL/CMOS

Note: 1. X = V_{IL} or V_{IH}.

Table 15. DC Characteristics
(T_A = 0 to 70°C, –20 to 85°C, –40 to 85°C; V_{CCF} = V_{CCS} = 2.7V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CCF}$ / V_{CCS}	–1	1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CCF}$ / V_{CCS}	–1	1	µA
I_{CCF1}	Flash Chip Supply Current (Read)	$\overline{EF} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz, $V \le V_{OUT} \le V_{CCF}$		10	mA
I_{CCF2} (1)	Flash Chip Supply Current (Write)	Program or Erase in progress		20	mA
I_{CCF3}	Flash Chip Supply Current (Stand-by)	$\overline{EF} = V_{CCF} \pm 0.2V$		100	µA
I_{CCS1}	SRAM Chip Supply Current (Read)	$\overline{E1S} = V_{IL}$, E2S = V_{IH}, f= 10MHz		40	mA
		$\overline{E1S} = V_{IL}$, E2S = V_{IH}, f= 1MHz		10	mA
I_{CCS2} (1)	SRAM Chip Supply Current (Write)			20	mA
I_{CCS3}	SRAM Chip Supply Current (Stand-by)			20	µA
V_{ILF}	Flash Chip Input Low Voltage		–0.5	0.8	V
V_{IHF}	Flash Chip Input High Voltage		0.7 V_{CCF}	V_{CCF} + 0.3	V
V_{ILS}	SRAM Chip Input Low Voltage		–0.3	0.4	V
V_{IHS}	SRAM Chip Input High Voltage		2.2	V_{CCS} + 0.3	V
V_{OLF}	Flash Chip Output Low Voltage	I_{OL} = 1.8mA		0.45	V
V_{OHF}	Flash Chip Output High Voltage	I_{OH} = –100µA	V_{CCF} – 0.4		V
V_{OLS}	SRAM Chip Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OHS}	SRAM Chip Output High Voltage	I_{OH} = –1.0mA	2.2		V

Note: 1. Sampled only, not 100% tested.

Table 16. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 17. AC Measurement Conditions

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Figure 5. AC Testing Input/Output Waveforms

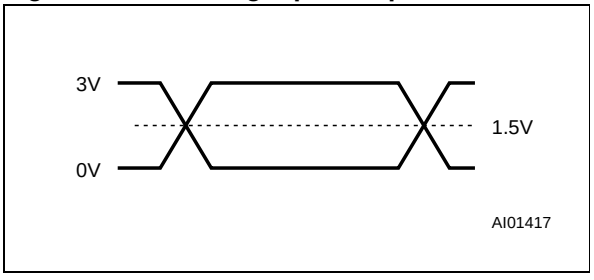


Figure 6. AC Testing Load Circuit

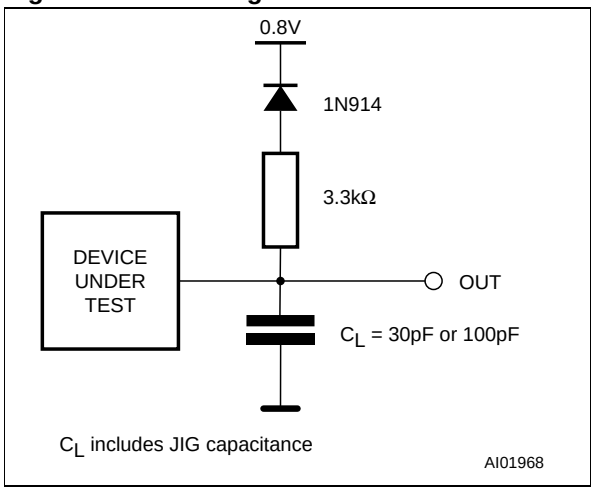


Table 18. Flash Read AC Characteristics
(T_A = 0 to 70 °C, –20 to 85 °C or –40 to 85 °C; V_{CCF} = 2.7V to 3.6V)

Symbol	Alt	Parameter	Test Condition	Flash Memory Chip				Unit
				100		120		
				C_L = 30pF		C_L = 100pF		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{EF}$ = V_{IL}, $\overline{G}$ = V_{IL}	100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{EF}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enabled Low to Output Transition	$\overline{EF}$ = V_{IL}	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{EF}$ = V_{IL}		40		50	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		30		30	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{EF}$ = V_{IL}	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{EF}$ = V_{IL}		30		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{EF}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns
t_{PLYH} (1,3)	t_{RRB} t_{READY}	$\overline{RP}$ Low to Read Mode			10		10	µs
t_{PHEL}	t_{RH}	$\overline{RP}$ High to Chip Enable Low		50		50		ns
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width		500		500		ns
t_{CCR} (4)		Chip Enabled Recovery Time		0		0		ns

Note: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{EF}$ without increasing t_{ELQV}.
3. To be considered only if the Reset pulse is given while the memory is in Erase, Erase Suspend or Program Mode.
4. See Flash-SRAM Switching Waveforms.

Figure 7. Flash Read Mode AC Waveforms

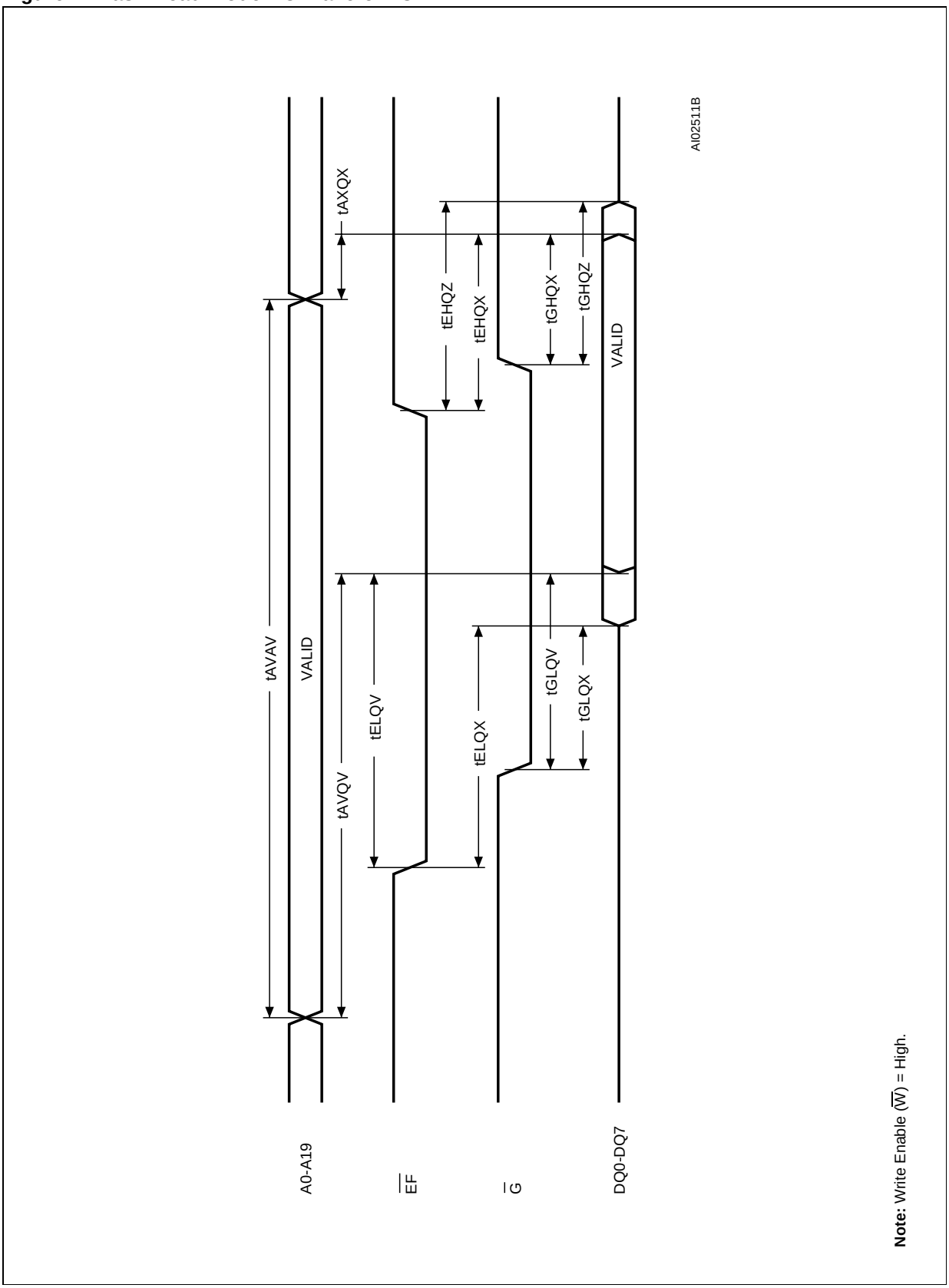
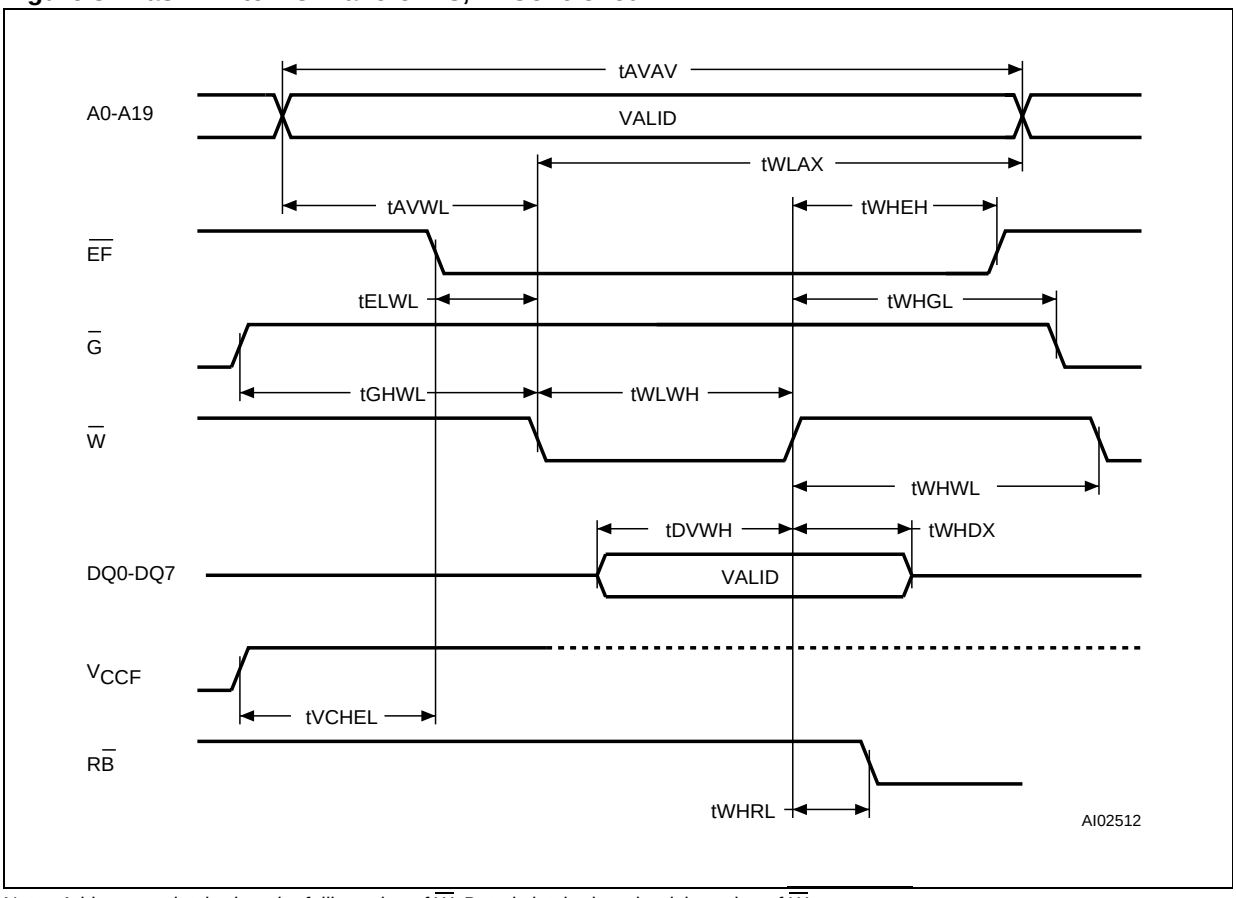


Table 19. Flash Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70 °C, –20 to 85 °C or –40 to 85 °C; V_{CCF} = 2.7V to 3.6V)

Symbol	Alt	Parameter	Flash Memory Chip				Unit
			100		120		
			C_L = 30pF		C_L = 100pF		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	100		120		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		50		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		30		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	50		50		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		µs
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns
t_{PHPHH} (1,2)	t_{VIDR}	$\overline{RP}$ Rise Time to V_{ID}	500		500		ns
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width	500		500		ns
t_{WHRL} (1)	t_{BUSY}	Program Erase Valid to $R\overline{B}$ Delay		90		90	ns
t_{PHWL} (1)	t_{RSP}	$\overline{RP}$ High to Write Enable Low	4		4		µs

Note: 1. Sampled only, not 100% tested.
2. This timing is for Temporary Block Unprotection operation.

Figure 8. Flash Write AC Waveforms, $\overline{W}$ Controlled



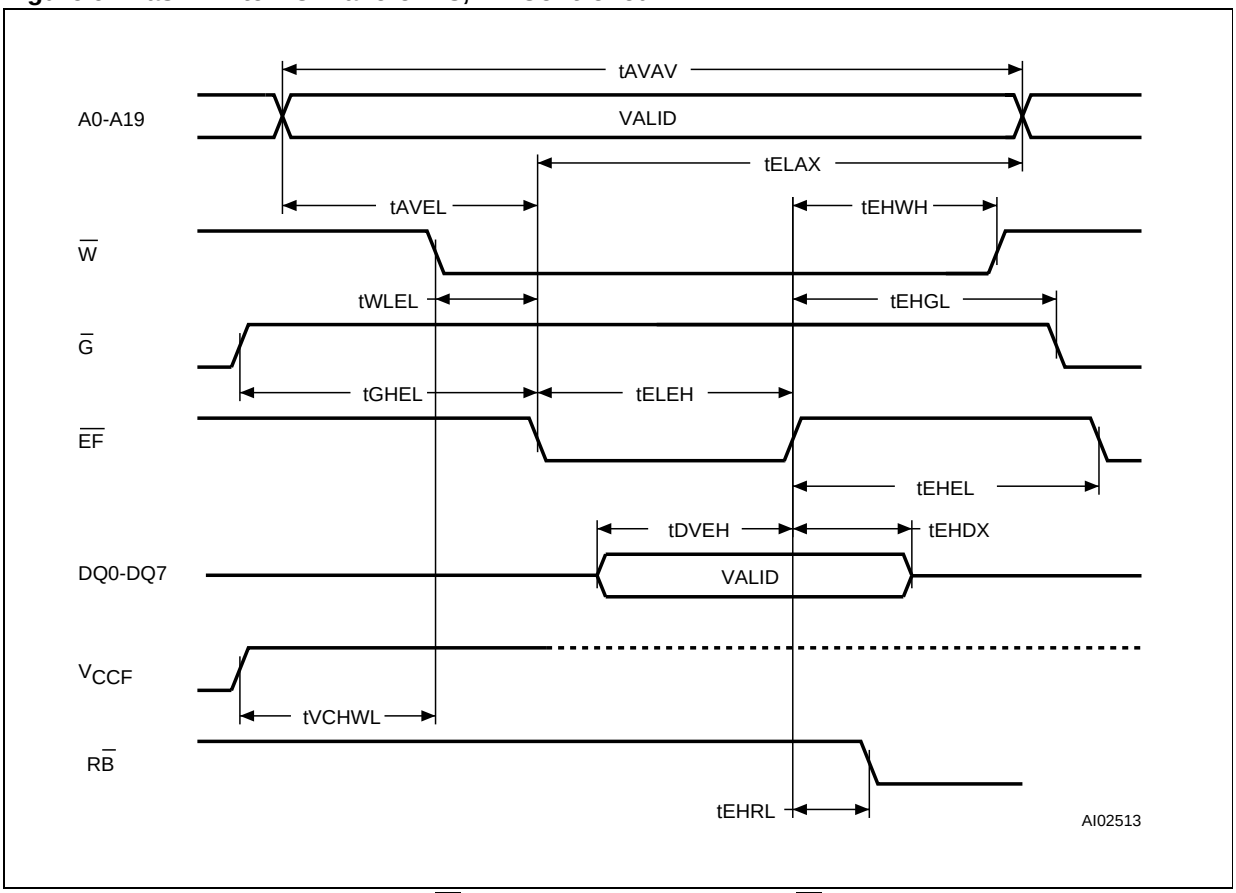
Note: Address are latched on the falling edge of $\overline{W}$, Data is latched on the rising edge of $\overline{W}$.

Table 20. Flash Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70 °C, –20 to 85 °C or –40 to 85 °C; V_{CCF} = 2.7V to 3.6V)

Symbol	Alt	Parameter	Flash Memory Chip				Unit
			100		120		
			C_L = 30pF		C_L = 100pF		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	100		120		ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	50		50		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	50		50		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	30		20		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	0		0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	50		50		ns
t_{GHEL}		Output Enable High Chip Enable Low	0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		µs
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	0		0		ns
t_{PHPHH} (1,2)	t_{VIDR}	$\overline{RP}$ Rise Time to V_{ID}	500		500		ns
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width	500		500		ns
t_{EHRL} (1)	t_{BUSY}	Program Erase Valid to R$\overline{B}$ Delay		90		90	ns
t_{PHWL} (1)	t_{RSP}	$\overline{RP}$ High to Write Enable Low	4		4		µs

Note: 1. Sampled only, not 100% tested.
2. This timing is for Temporary Block Unprotection operation.

Figure 9. Flash Write AC Waveforms, $\overline{EF}$ Controlled



Note: Address are latched on the falling edge of $\overline{EF}$, Data is latched on the rising edge of $\overline{EF}$.

Figure 10. Flash Read and Write AC Waveforms, $\overline{RP}$ Related

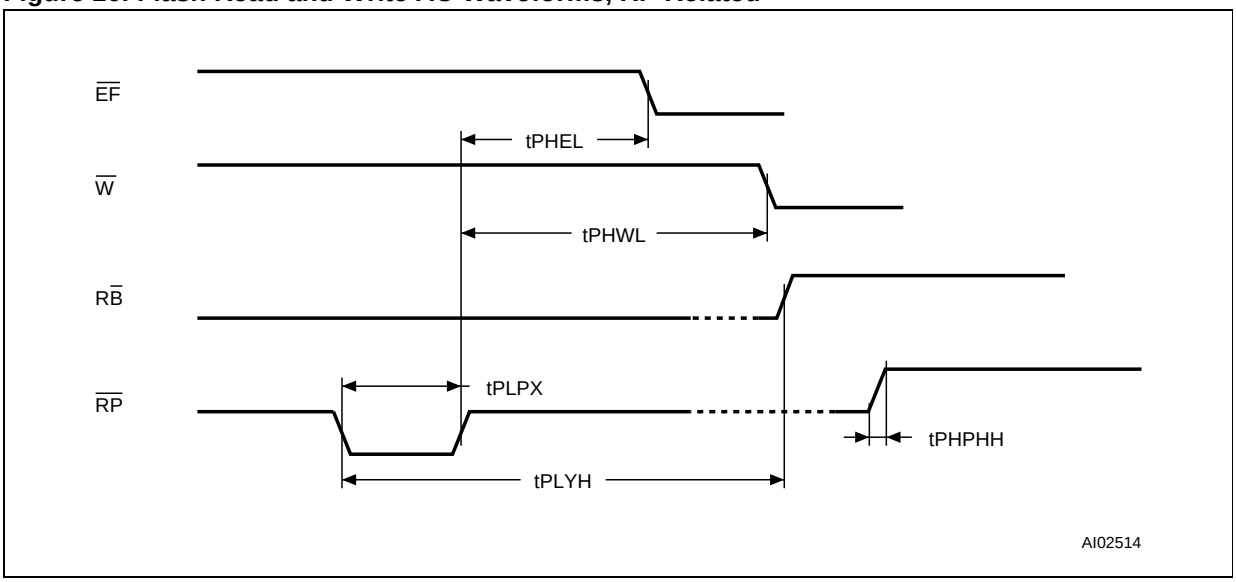


Table 21. Flash Data Polling and Toggle Bits AC Characteristics (1)
(T_A = 0 to 70 °C, –20 to 85 °C or –40 to 85 °C; V_{CCF} = 2.7V to 3.6V)

Symbol	Parameter	Flash Memory Chip				Unit
		100		120		
		C_L = 30pF		C_L = 100pF		
		Min	Max	Min	Max	
t_{WHQ7V}	Write Enable High to DQ7 Valid (Program, $\overline{W}$ Controlled)	10	2400	10	2400	ms
	Write Enable High to DQ7 Valid (Chip Erase, $\overline{W}$ Controlled)	1.0	60	1.0	60	sec
t_{EHQ7V}	Chip Enable High to DQ7 Valid (Program, $\overline{EF}$ Controlled)	10	2400	10	2400	µs
	Chip Enable High to DQ7 Valid (Chip Erase, $\overline{EF}$ Controlled)	1.0	60	1.0	60	sec
t_{Q7VQV}	Q7 Valid to Output Valid (Data Polling)		40		50	ns
t_{WHQV}	Write Enable High to Output Valid (Program)	10	2400	10	2400	µs
	Write Enable High to Output Valid (Chip Erase)	1.0	60	1.0	60	sec
t_{EHQV}	Chip Enable High to Output Valid (Program)	10	2400	10	2400	µs
	Chip Enable High to Output Valid (Chip Erase)	1.0	60	1.0	60	sec

Note: 1. All other timings are defined in Read AC Characteristics table.

Figure 11. Flash Data Polling DQ7 AC Waveforms

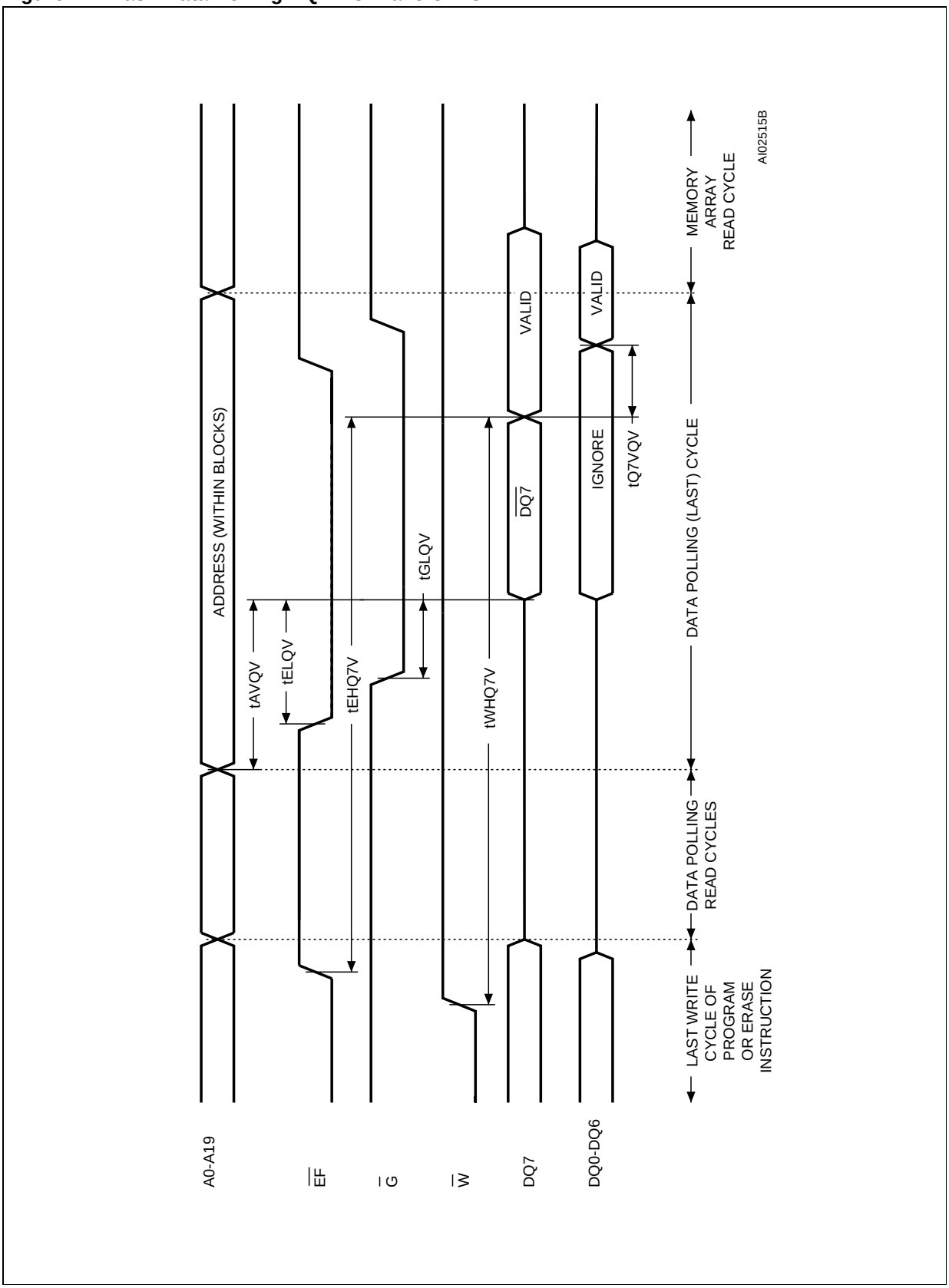


Figure 12. Flash Data Toggle DQ6, DQ2 AC Waveforms

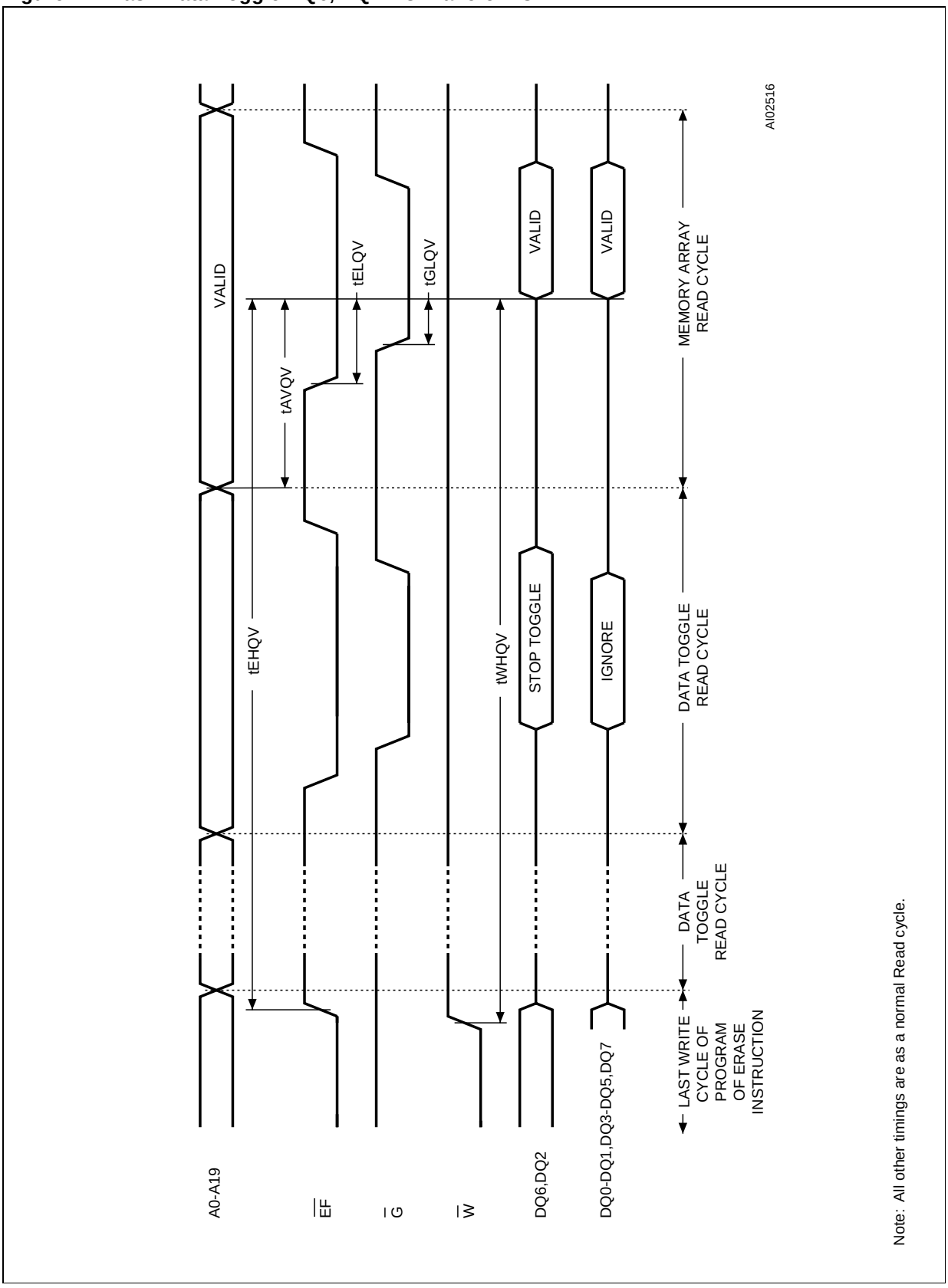


Figure 13. Flash Data Polling Flowchart

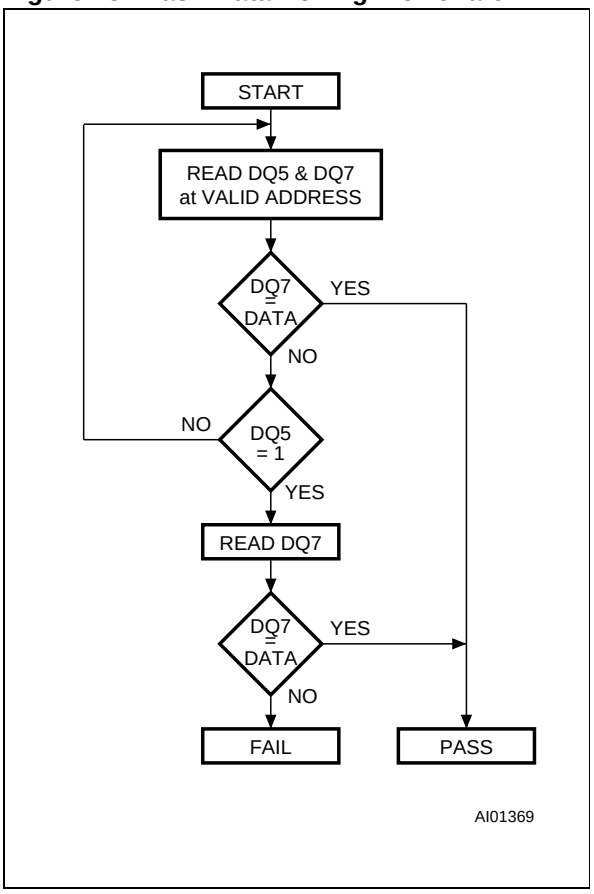


Figure 14. Flash Data Toggle Flowchart

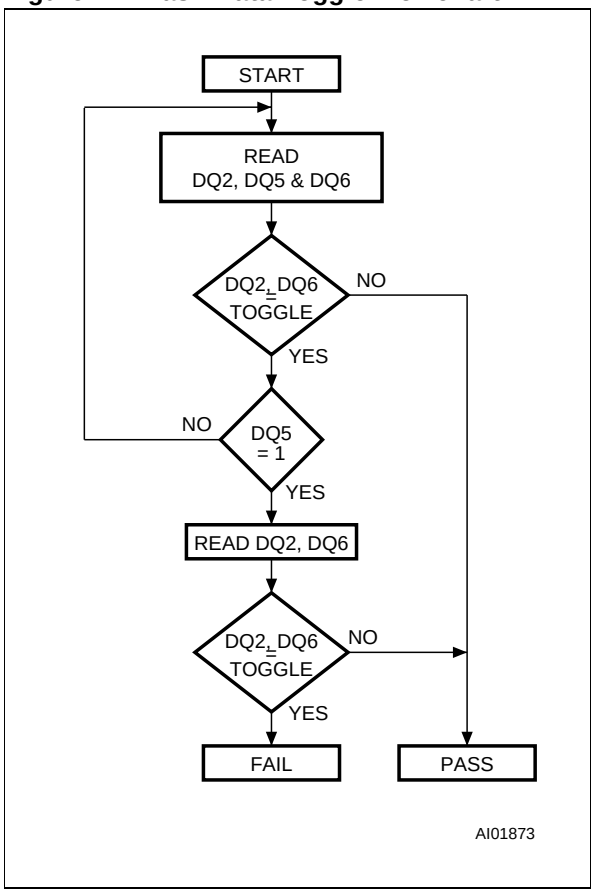
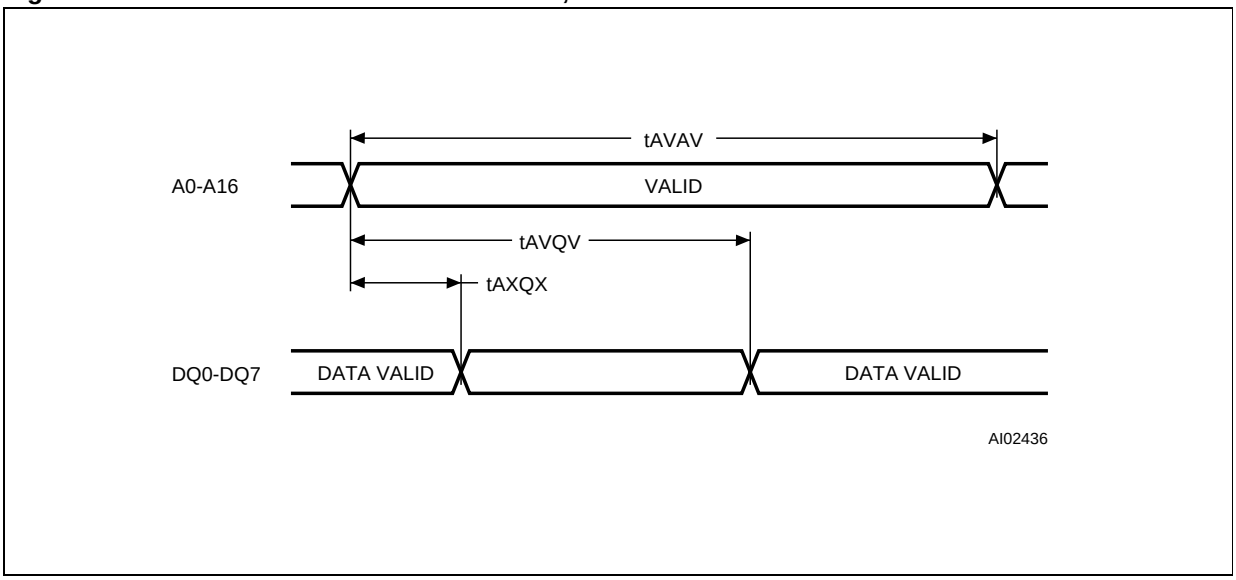


Table 22. SRAM Read AC Characteristics
(T_A = 0 to 70 °C, –20 to 85 °C or –40 to 85 °C; V_{CCS} = 2.7 V to 3.6 V)

Symbol	Parameter	SRAM Chip		Unit
		100		
		C_L = 100pF		
		Min	Max	
t_{AVAV}	Read Cycle Time	100		ns
t_{AVQV}	Address Valid to Output Valid		100	ns
t_{E1LQV}	Chip Enable 1 Low to Output Valid		100	ns
t_{E2HQV}	Chip Enable 2 High to Output Valid		100	ns
t_{GLQV}	Output Enable Low to Output Valid		50	ns
t_{E1LQX}	Chip Enable 1 Low to Output Transition	10		ns
t_{E2HQX}	Chip Enable 2 High to Output Transition	10		ns
t_{GLQX}	Output Enable Low to Output Transition	5		ns
t_{E1HQZ}	Chip Enable 1 High to Output Hi-Z	0	30	ns
t_{E2LQZ}	Chip Enable 2 Low to Output Hi-Z	0	30	ns
t_{GHQZ}	Output Enable High to Output Hi-Z	0	30	ns
t_{AXQX}	Address Transition to Output Transition	15		ns
t_{PU} (1)	Chip Enable 1 Low or Chip Enable 2 High to Power Up	0		ns
t_{PD} (1)	Chip Enable 1 High or Chip Enable 2 Low to Power Down		100	ns
t_{CCR} (2)	Chip Enable Recovery Time	0		ns

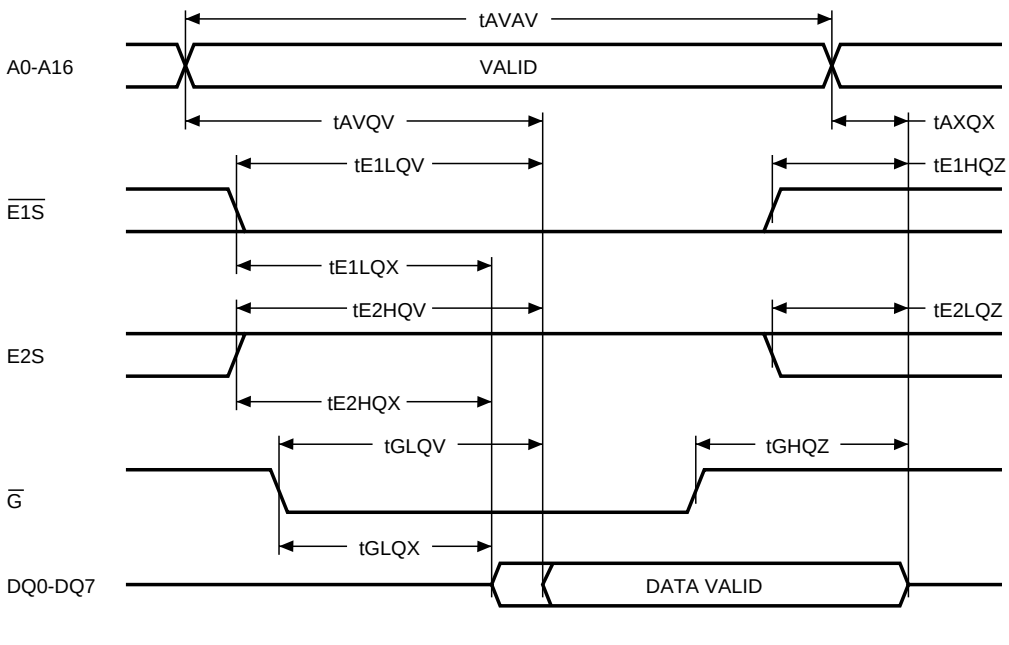
Note: 1. Sampled only. Not 100% tested.
2. See Flash-SRAM Switching Waveforms.

Figure 15. SRAM Read Mode AC Waveforms, Address Controlled



Note: $\overline{E1S}$ = Low, E2S = High, $\overline{G}$ = Low, $\overline{W}$ = High.

Figure 16. SRAM Read AC Waveforms, $\overline{E1S}$, E2S or $\overline{G}$ Controlled



Note: Write Enable ($\overline{W}$) = High.

Figure 17. SRAM Stand-by AC Waveforms

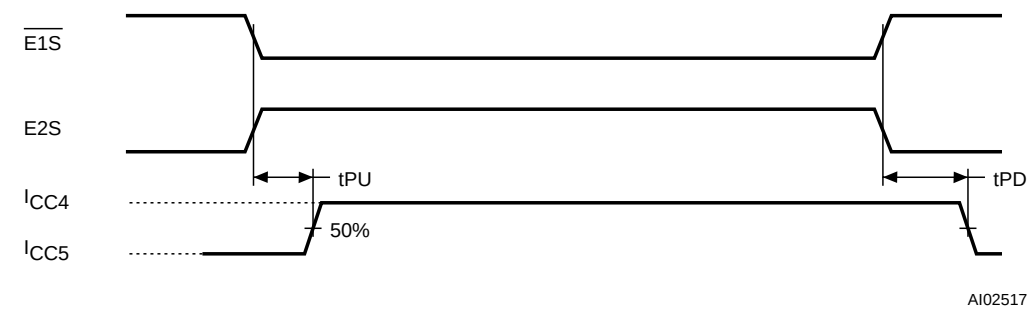
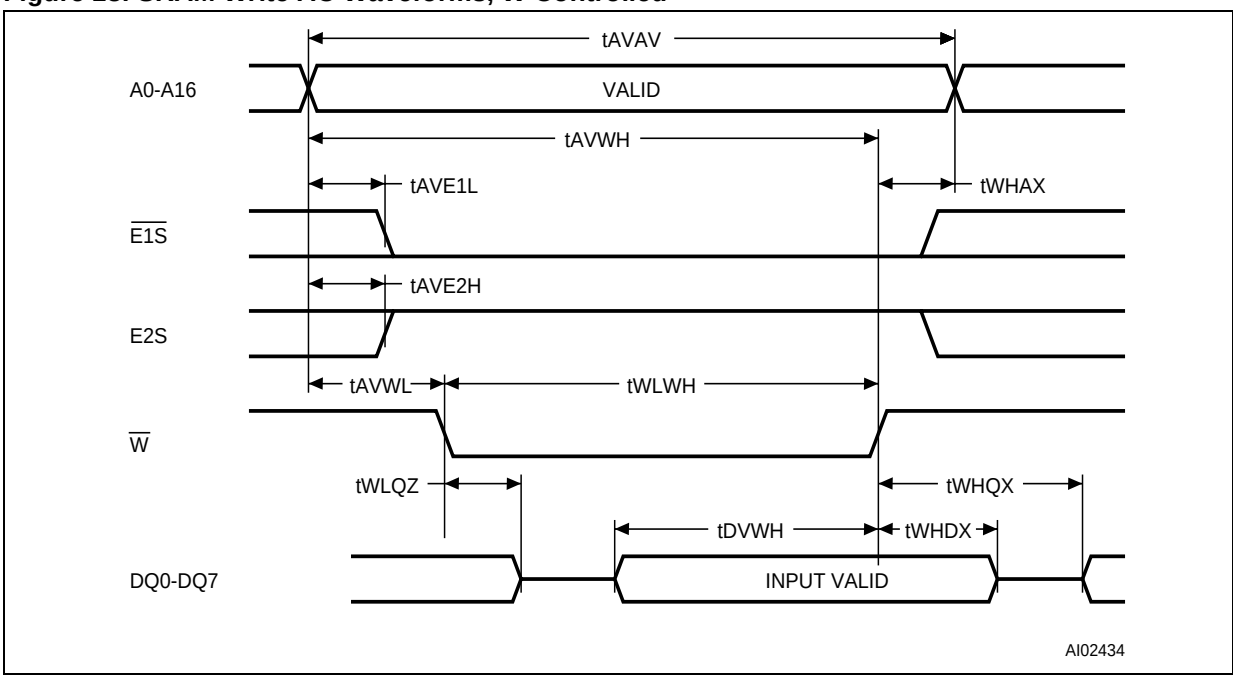


Table 23. SRAM Write AC Characteristics
(T_A = 0 to 70 °C, –20 to 85 °C or –40 to 85 °C; V_{CCS} = 2.7 V to 3.6 V)

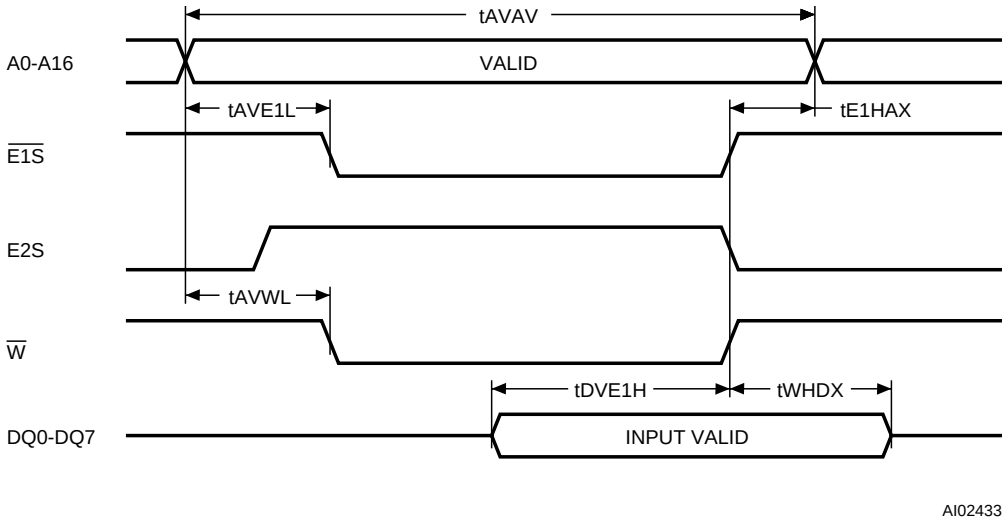
Symbol	Parameter	SRAM Chip		Unit
		100		
		C_L = 100pF		
		Min	Max	
t_{AVAV}	Write Cycle Time	100		ns
t_{AVWL}	Address Valid to Write Enable Low	0		ns
t_{AVWH}	Address Valid to Write Enable High	80		ns
t_{WLWH}	Write Enable Pulse Width	70		ns
t_{WHAX}	Write Enable High to Address Transition	0		ns
t_{WHDX}	Write Enable High to Input Transition	0		ns
t_{WHQX}	Write Enable High to Output Transition	0		ns
t_{WLQZ}	Write Enable Low to Output Hi-Z	0	30	ns
t_{AVE1L}	Address Valid to Chip Enable 1 Low	0		ns
t_{AVE2H}	Address Valid to Chip Enable 2 High	0		ns
t_{E1HAX}	Chip Enable 1 High to Address Transition	0		ns
t_{E2LAX}	Chip Enable 2 Low to Address Transition	0		ns
t_{DVWH}	Input Valid to Write Enable High	40		ns
t_{DVE1H}	Input Valid to Chip Enable 1 High	40		ns
t_{DVE2L}	Input Valid to Chip Enable 2 Low	40		ns

Figure 18. SRAM Write AC Waveforms, $\overline{W}$ Controlled



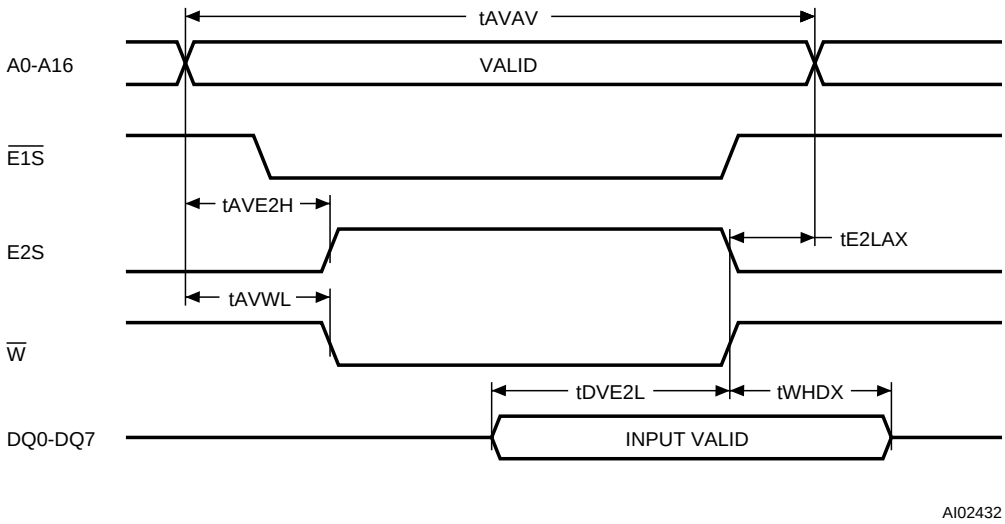
Note: Output Enable ($\overline{G}$) = Low.

Figure 19. SRAM Write AC Waveforms, $\overline{E1S}$ Controlled



Note: Output Enable ($\overline{G}$) = High.

Figure 20. SRAM Write AC Waveforms, E2S Controlled



Note: Output Enable ($\overline{G}$) = High.

Table 24. SRAM Low V_{CC} Data Retention Characteristics (1, 2)
(T_A = 0 to 70 °C; V_{CCS} = 2.7 V to 3.6 V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{CCDR}	Supply Current (Data Retention)	V_{CCS} = 3V, $\overline{E1S} \geq V_{CCS} - 0.2V$, E2S ≥ V_{CCS} – 0.2V or E2S ≤ 0.2V, f = 0		20	µA
V_{DR}	Supply Voltage (Data Retention)	$\overline{E1S} \geq V_{CCS} - 0.2V$,E2S ≤ 0.2V, f = 0	2	3.6	V
t_{CDR}	Chip Disable to Power Down	$\overline{E1S} \geq V_{CCS} - 0.2V$,E2S ≤ 0.2V, f = 0	0		ns
t_R	Operation Recovery Time		5		ms

Note: 1. All other Inputs $V_{IH} \leq V_{CC} - 0.2V$ or $V_{IL} \leq 0.2V$.
2. Sampled only. Not 100% tested.

Figure 21. SRAM Low V_{CC} Data Retention AC Waveforms, $\overline{E1S}$ Controlled

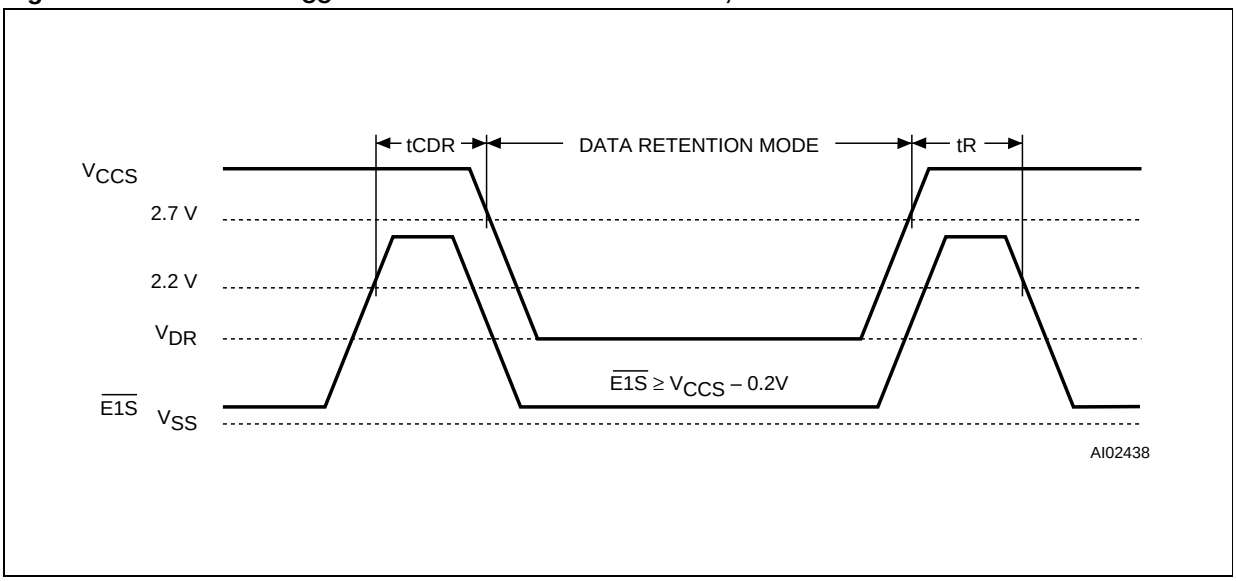


Figure 22. SRAM Low V_{CC} Data Retention AC Waveforms, E2S Controlled

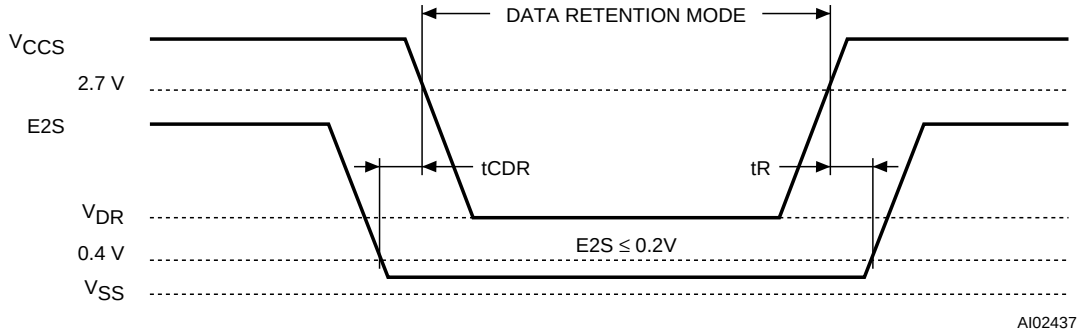


Figure 23. Flash-SRAM Switching Waveforms

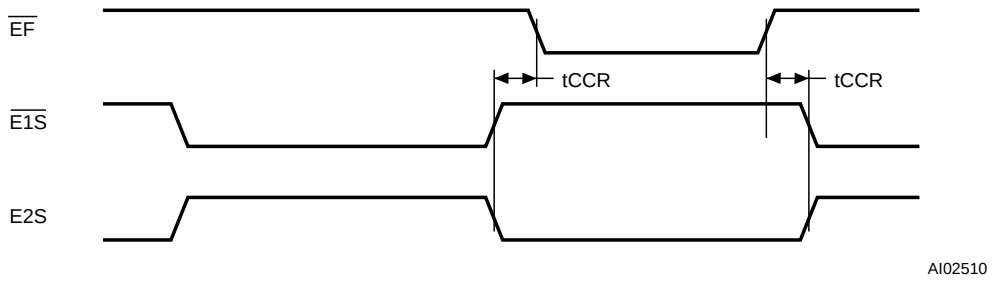


Table 25. Ordering Information Scheme

Example: M36W108AT 100 ZM 1 T

Product Family
M36 = MMP (Flash + SRAM)

Operating Voltage
W = 2.7V to 3.6V

SRAM Chip size & organization
1 = 1 Mbit (x8)

Flash Chip size & orgnization
08A = 8 Mbit (x8)

Array Matrix
T = Top Boot
B = Bottom Boot

Speed
100 = 100 ns
120 = 120 ns

Package
ZM = LBGA48: 1mm pitch
ZN = LGA48: 1mm pitch

Temperature Range
1 = 0 to 70 °C
5 = –20 to 85 °C
6 = –40 to 85 °C

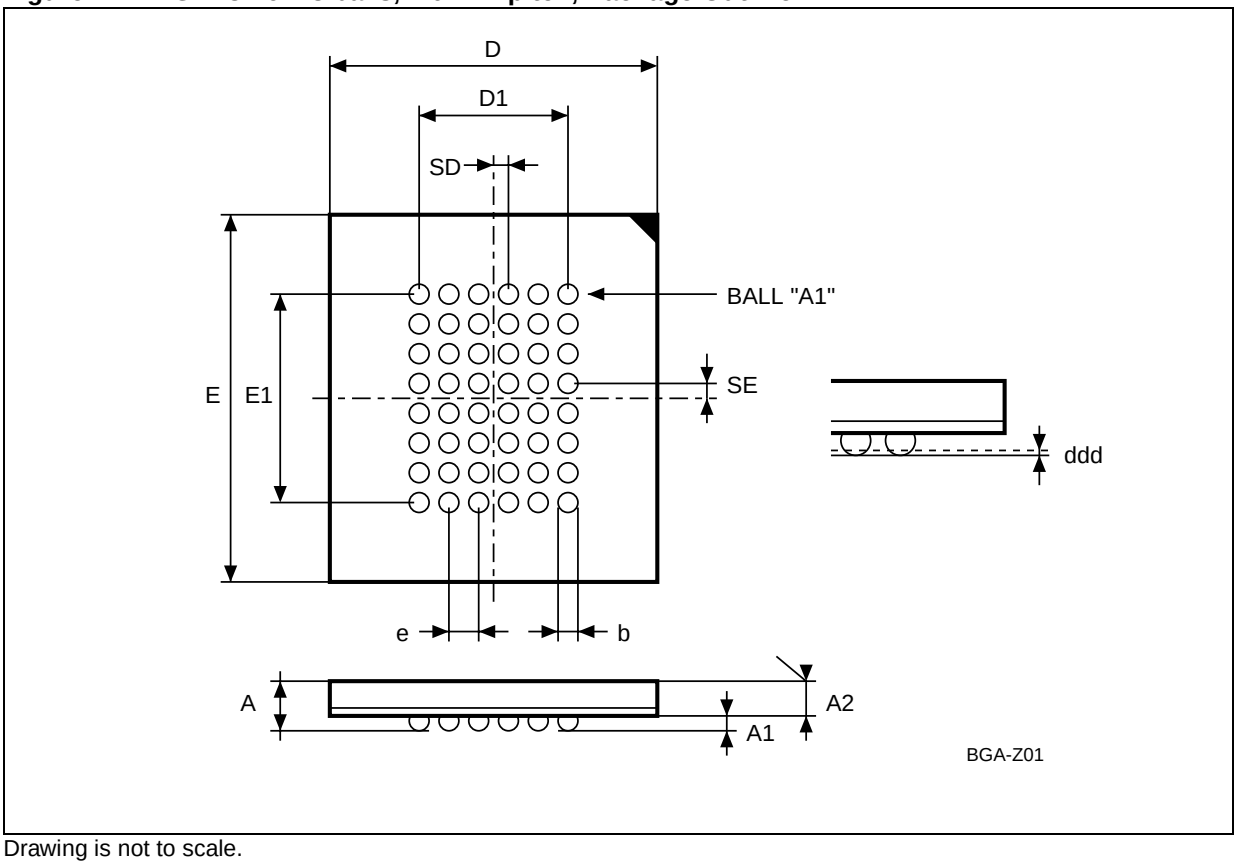
Option
T = Tape & Reel Packing

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 26. LBGA48 - 6 x 8 balls, 1.0 mm pitch, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	1.250	1.150	1.350	0.049	0.045	0.053
A1	0.300	0.250	0.350	0.012	0.010	0.014
A2	0.950	–	–	0.037	–	–
b	0.400	0.350	0.450	0.016	0.014	0.018
ddd			0.150			0.006
D	10.000	9.800	10.200	0.394	0.386	0.402
D1	5.000	–	–	0.197	–	–
e	1.000	–	–	0.039	–	–
E	12.000	11.800	12.200	0.472	0.465	0.480
E1	7.000	–	–	0.276	–	–
SD	0.500	–	–	0.020	–	–
SE	0.500	–	–	0.020	–	–

Figure 24. LBGA48 - 6 x 8 balls, 1.0 mm pitch, Package Outline

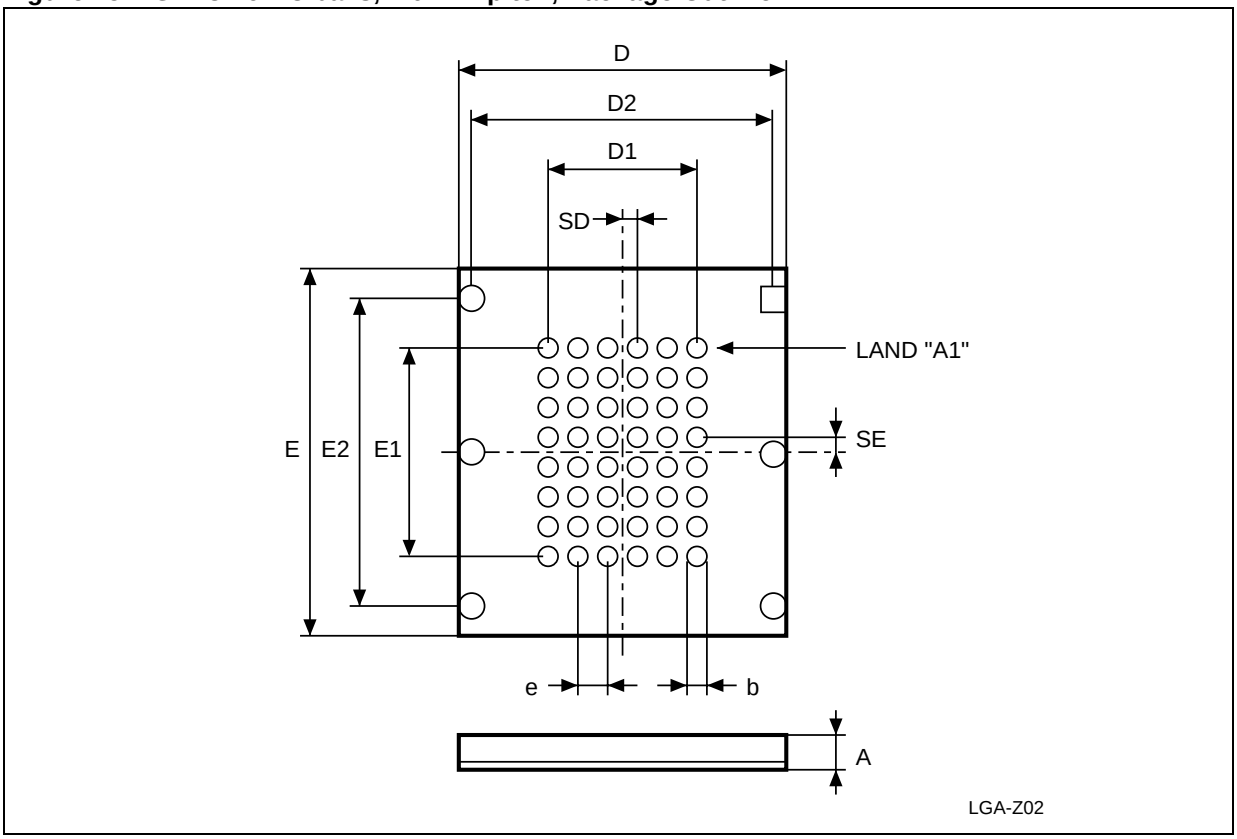


Drawing is not to scale.

Table 27. LGA48 - 6 x 8 balls, 1.0 mm pitch, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	0.950	0.900	1.000	0.037	0.035	0.039
b	0.450	0.420	0.480	0.018	0.017	0.019
D	10.000	9.800	10.200	0.394	0.386	0.402
D1	5.000	–	–	0.197	–	–
D2	9.200	–	–	0.362	–	–
e	1.000	–	–	0.039	–	–
E	12.000	11.800	12.200	0.472	0.465	0.480
E1	7.000	–	–	0.276	–	–
E2	10.200	–	–	0.402	–	–
SD	0.500	–	–	0.020	–	–
SE	0.500	–	–	0.020	–	–

Figure 25. LGA48 - 6 x 8 balls, 1.0 mm pitch, Package Outline



Drawing is not to scale.

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